SRI MANAKULA VINAYAGAR
ENGINEERING COLLEGE
(AN AUTONOMOUS INSTITUTION)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CURRICULUM & SYLLABI
(Regulations 2023)

M.Tech - VLSI and Embedded Systems

SRI MANAKULA VINAYAGAR
ENGINEERING COLLEGE
(AN AUTONOMOUS INSTITUTION)

M.TECH.

VLSI AND EMBEDDED SYSTEMS

(Regulations-2023)

CURRICULUM & SYLLABI

A

VISION AND MISSION OF THE INSTITUTE

VISION

To be globally recognized for excellence in quality education, innovation, and research for the transformation of lives to serve the society.

MISSION

M1: Quality Education	To provide comprehensive academic system that amalgamates the cutting edge-technologies with best practices
M2: Research and Innovation	To foster value-based research and innovation in collaboration with industries and institutions globally for creating intellectuals with new avenues
M3: Employability and Entrepreneurship	To inculcate the employability and entrepreneurial skills through value and skill-based training
M4: Ethical Values	To instil deep sense of human values by blending societal righteousness with academic professionalism for the growth of society

VISION AND MISSION OF THE DEPARTMENT

VISION

Facilitate academic excellence and research among Electronics and Communication Engineers to meet the Global needs with high competence and ethical professionalism

MISSION

M1: Academic Excellence	To impart learning skills to meet the global challenges in the field of Electronics and Communication Engineering
M2: Research and Innovation	To provide excellence in research and innovation through multidisciplinary specialization
M3: Employability and Entrepreneurship	To enhance inter and intrapersonal skills among students to make them employable and entrepreneurs
M4: Ethics	To inculcate the significance of human values and professional skills to serve the society

PROGRAMME OUTCOMES (POs)

PO1: Engineering knowledge:

Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis:

Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/development of solutions:

Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems:

Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage:

Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society:

Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability:

Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.

PO8: Ethics:

Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and teamwork:

Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication:

Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance:

Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning:

Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM EDUCATIONAL OBCTIVES (PEOs)

PEO1: Technical Knowledge
Graduates will be able to develop an insightful combination of modern electronics and communication technology through technical knowledge.

PEO2: Research and Development
Enhance analytical and thinking skills to develop initiatives and innovative ideas for research and development, industry, and societal requirements.

PEO3: Leadership
Inculcate the qualities of teamwork as well as social, interpersonal and leadership skills and adapt to the changing professional environments in the fields of engineering and technology.

PEO4: Professional Ethics
Motivate graduates to become good human beings and responsible citizens for the overall welfare of the society.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Domain Knowledge
Ability to understand the concepts in Electronics and Communication Engineering and to apply to different fields, such as Consumer Electronics, Communications, Signal Processing, etc.

PSO2: Embedded System Design
Ability to design a system based on the technical knowledge gained for embedded applications in electronics and communications engineering.

PSO3: Professional Competency
Ability to select cutting-edge engineering hardware and software tools to solve complex problems in Electronics and Communication Engineering

STRUCTURE FOR POSTGRADUATE ENGINEERING PROGRAM

S.No	Category	Credits
1	Humanities and Social Sciences including Management courses	6
2	Basic Science courses	3
4	Professional core courses	25
5	Professional Elective courses	18
6	Project work, and internship	20
7	Ability Enhancement Courses	
Total Credits		**72**

SCHEME OF CREDIT DISTRIBUTION – SUMMARY

S. No	Category	Credits per Semester				Total credits
		I	II	III	IV	
1	Humanities and Social Sciences including Management courses	4	2			6
2	Basic Science courses	3				3
4	Professional Core courses	11	14			25
5	Professional Elective courses	3	6	9		18
6	Project work and internship			8	12	20
7	Ability Enhancement Courses*					
Total Credits		21	22	17	12	72

* AEC is not included for CGPA calculation

SEMESTER–I

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23MAT102	Applied Mathematics for VLSI	BS	2	2	0	3	40	60	100
2	P23VET101	Electronic Design Automation Tools	PC	3	0	0	3	40	60	100
3	P23VET102	FPGA Based System Design	PC	3	0	0	3	40	60	100
4	P23VET103	VLSI Design Techniques	PC	3	0	0	3	40	60	100
5	P23HSTC01	Research Methodology and IPR	HS	2	0	0	2	40	60	100
6	P23VEE1XX	Professional Elective - I	PE	3	0	0	3	40	60	100
Practical										
7	P23VEP101	VLSI Design Laboratory	PC	0	0	4	2	50	50	100
8	P23HSPC02	Technical Report Writing and Seminar	HS	0	0	4	2	100	0	100
Ability Enhancement Course										
9	P23VEC1XX	Certification Course - I	AEC	0	0	4	-	100	-	100
10	P23ACT10X	Audit Course - I	AEC	2	0	0	-	100	-	100
							21	**590**	**410**	**1000**

SEMESTER–II

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23VETC01	Advanced Digital System Design	PC	3	0	0	3	40	60	100
2	P23VETC02	Embedded Processors	PC	3	0	0	3	40	60	100
3	P23VETC03	Embedded System Design	PC	3	0	0	3	40	60	100
4	P23VET204	Low Power Digital VLSI Design	PC	3	0	0	3	40	60	100
5	P23VEE2XX	Professional Elective - II	PE	3	0	0	3	40	60	100
6	P23VEE2XX	Professional Elective - III	PE	3	0	0	3	40	60	100
Practical										
7	P23VEP202	Embedded System Design Laboratory	PC	0	0	4	2	50	50	100
8	P23HSPC03	Seminar on ICT a hands-on approach	HS	0	0	4	2	100	0	100
Ability Enhancement Course										
10	P23VEC2XX	Certification Course – II	AEC	0	0	4	-	100	-	100
11	P23ACT20X	Audit Course - II	AEC	2	0	0	-	100	-	100
Total							**22**	**590**	**410**	**1000**

SEMESTER–III

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23VEE3XX	Professional Elective - IV	PE	3	0	0	3	40	60	100
2	P23VEE3XX	Professional Elective - V	PE	3	0	0	3	40	60	100
3	P23VEE3XX	Professional Elective - VI	PE	3	0	0	3	40	60	100
Project Work										
4	P23VEW301	Project Phase - I	PA	0	0	12	6	50	50	100
5	P23VEW302	Internship	PA	0	0	0	2	100	0	100
Ability Enhancement Course										
6	P23VEC301	NPTEL / SWAYAM / MOOC	AEC	0	0	0	-	100	0	100
Total							**17**	**370**	**230**	**600**

SEMESTER–IV

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Project Work										
1	P23VEW403	Project Phase - II	PA	0	0	24	12	50	50	100
Total							**12**	**50**	**50**	**100**

* Professional Elective Courses are to be selected from the list given in Annexure I
# Ability Enhancement Courses are to be selected from the list given in Annexure II
** Audit Courses are to be selected from the list given in Annexure III

BS - Basic Science
HS - Humanity Science
PC - Professional Core
PE - Professional Elective
PA - Project Work
C - Common Course
AEC - Audit Course
AEC - Ability Enhancement Course

Credit Distribution

Semester- I	Semester - II	Semester - III	Semester - IV	Total
21	22	17	12	72

Total number of credits required to complete M. Tech - VLSI AND Embedded Systems: 72 credits

Annexure – I

PROFESSIONAL ELECTIVE COURSES

Professional Elective -I (Offered in Semester I)		
Sl. No.	**Course Code**	**Course Title**
1	P23VEE101	Principles of ASIC Design
2	P23VEE102	VLSI Architecture
3	P23VEE103	Physical Design of VLSI
4	P23VEE104	Real Time Systems
5	P23VEE105	Analog IC Design
Professional Elective - II (Offered in Semester II)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC01	Design of Analog and Mixed VLSI Circuits
2	P23VEEC02	Internet of Things and its Implementation
3	P23VEE206	Modeling and Synthesis with Verilog HDL
4	P23VEE207	Advanced Embedded System
5	P23VEE208	Distributed Embedded Computing
Professional Elective -III (Offered in Semester II)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC03	System-on-Chip Design
2	P23VEE209	DSP Processor Architecture and Programming
3	P23VEE210	Design for Verification Using UVM
4	P23VEE211	Testing and Fault Diagnosis of VLSI Circuits
5	P23VEE212	Soft Computing
Professional Elective-IV (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC04	Real Time Operating System
2	P23VEEC05	Cloud computing and Distributed System
3	P23VEE313	VLSI Signal Processing
4	P23VEE314	High Speed Digital Design
5	P23VEE315	Nanoelectronics
Professional Elective -V (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC06	Edge Computing
2	P23VEE316	CAD for VLSI Circuits
3	P23VEE317	Advanced Image Processing
4	P23VEE318	Hardware Software Co-Design
5	P23VEE319	Micro-Electromechanical Systems
Professional Elective-VI (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEE320	Smart Technologies for Pervasive Computing
2	P23VEE321	Robotics and Automation
3	P23VEE322	Semiconductor Devices and Modeling
4	P23VEE323	VLSI for Wireless Communication
5	P23VEE324	RISC Processor Architecture and Programming

Annexure – II

ABILITY ENHANCEMENT COURSES

Sl. No.	Course Code	Course Title
1	P23ECCX01	Adobe Photoshop
2	P23ECCX02	Adobe Animate
3	P23ECCX03	Adobe Dreamweaver
4	P23ECCX04	Adobe After Effects
5	P23ECCX05	Adobe Illustrator
6	P23ECCX06	Adobe InDesign
7	P23ECCX07	Autodesk AutoCAD -ACU
8	P23ECCX08	Autodesk Inventor - ACU
9	P23ECCX09	Autodesk Revit - ACU
10	P23ECCX10	Autodesk Fusion 360 - ACU
11	P23ECCX11	Autodesk 3ds Max - ACU
12	P23ECCX12	Autodesk Maya - ACU
13	P23ECCX13	Cloud Security Foundations
14	P23ECCX14	Cloud Computing Architecture
15	P23ECCX15	Cloud Foundation
16	P23ECCX16	Cloud Practitioner
17	P23ECCX17	Cloud Solution Architect
18	P23ECCX18	Data Engineering
19	P23ECCX19	Machine Learning Foundation
20	P23ECCX20	Robotic Process Automation / Medical Robotics
21	P23ECCX21	Advance Programming Using C
22	P23ECCX22	Advance Programming Using C ++
23	P23ECCX23	C Programming
24	P23ECCX24	C++ Programming
25	P23ECCX25	CCNP Enterprise: Advanced Routing
26	P23ECCX26	CCNP Enterprise: Core Networking
27	P23ECCX27	Cisco Certified Network Associate - Level 2

28	P23ECCX28	Cisco Certified Network Associate- Level 1
29	P23ECCX29	Cisco Certified Network Associate- Level 3
30	P23ECCX30	Fundamentals Of Internet of Things
31	P23ECCX31	Python Programming
32	P23ECCX32	Java Script Programming
33	P23ECCX33	NGD Linux Essentials
34	P23ECCX34	NGD Linux I
35	P23ECCX35	NGD Linux II
36	P23ECCX36	Advance Java Programming
37	P23ECCX37	Android Programming / Android Medical App Development
38	P23ECCX38	Angular JS
39	P23ECCX39	Catia
40	P23ECCX40	Communication Skills for Business
41	P23ECCX41	Coral Draw
42	P23ECCX42	Data Science Using R
43	P23ECCX43	Digital Marketing
44	P23ECCX44	Embedded System Using C
45	P23ECCX45	Embedded System with IOT / Arduino
46	P23ECCX46	English For IT
47	P23ECCX47	Plaxis
48	P23ECCX48	Sketch Up
49	P23ECCX49	Financial Planning, Banking and Investment Management
50	P23ECCX50	Foundation Of Stock Market Investing
51	P23ECCX51	Machine Learning / Machine Learning for Medical Diagnosis
52	P23ECCX52	IOT Using Python
53	P23ECCX53	Creo (Modelling & Simulation)
54	P23ECCX54	Soft Skills, Verbal, Aptitude
55	P23ECCX55	Software Testing
56	P23ECCX56	MX-Road
57	P23ECCX57	CLO 3D
58	P23ECCX58	Solid works

59	P23ECCX59	Staad Pro
60	P23ECCX60	Total Station
61	P23ECCX61	Hydraulic Automation
62	P23ECCX62	Industrial Automation
63	P23ECCX63	Pneumatics Automation
64	P23ECCX64	Agile Methodologies
65	P23ECCX65	Block Chain
66	P23ECCX66	Devops
67	P23ECCX67	Artificial Intelligence
68	P23ECCX68	Cloud Computing
69	P23ECCX69	Computational Thinking
70	P23ECCX70	Cyber Security
71	P23ECCX71	Data Analytics
72	P23ECCX72	Databases
73	P23ECCX73	Java Programming
74	P23ECCX74	Networking
75	P23ECCX75	Internet Of Things / Solar and Smart Energy System with IoT
76	P23ECCX76	Web Application Development (HTML, CSS, JS)
77	P23ECCX77	Network Security
78	P23ECCX78	MATLAB
79	P23ECCX79	Azure Fundamentals
80	P23ECCX80	Azure AI (AI-900)
81	P23ECCX81	Azure Data (DP -900)
82	P23ECCX82	Microsoft 365 Fundamentals (SS-900)
83	P23ECCX83	Microsoft Security, Compliance and Identity (SC-900)
84	P23XXCX84	Microsoft Power Platform (PI-900)
85	P23XXCX85	Microsoft Dynamics Fundamentals 365 – CRM
86	P23XXCX86	Microsoft Excel
87	P23XXCX87	Microsoft Excel Expert
88	P23XXCX88	Securities Market Foundation
89	P23XXCX89	Derivatives Equinity

90	P23XXCX90	Research Analyst
91	P23XXCX91	Portfolio Management Services
92	P23XXCX92	Cyber Security
93	P23XXCX93	Cloud Security
94	P23XXCX94	PMI - Ready
95	P23XXCX95	Tally - GST & TDS
96	P23XXCX96	Advance Tally
97	P23XXCX97	Associate Artist
98	P23XXCX98	Certified Unity Programming
99	P23XXCX99	VR Development

*66*Any one course to be selected from the list*

Annexure - III

AUDIT COURSES

Sl. No.	Course Code	Course Title
1	P23ACTX01	English for Research Paper Writing
2	P23ACTX02	Disaster Management
3	P23ACTX03	Sanskrit for Technical Knowledge
4	P23ACTX04	Value Education
5	P23ACTX05	Constitution of India
6	P23ACTX06	Pedagogy Studies
7	P23ACTX07	Stress Management by Yoga
8	P23ACTX08	Personality Development Through Life Enlightenment Skills
9	P23ACTX09	Unnat Bharat Abhiyan

SEMESTER – I

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23MAT102	Applied Mathematics for VLSI	BS	2	2	0	3	40	60	100
2	P23VET101	Electronic Design Automation Tools	PC	3	0	0	3	40	60	100
3	P23VET102	FPGA Based System Design	PC	3	0	0	3	40	60	100
4	P23VET103	VLSI Design Techniques	PC	3	0	0	3	40	60	100
5	P23HSTC01	Research Methodology and IPR	HS	2	0	0	2	40	60	100
6	P23VEE1XX	Professional Elective - I	PE	3	0	0	3	40	60	100
Practical										
7	P23VEP101	VLSI Design Laboratory	PC	0	0	4	2	50	50	100
8	P23HSPC01	Technical Report Writing and Seminar	HS	0	0	4	2	100	-	100
Ability Enhancement Course										
9	P23ECC1XX	Certification Course – I	AEC	0	0	4	-	100	-	100
10	P23ACT10X	Audit Course - I	AEC	2	0	0	-	100	-	100
Total							**21**	**590**	**410**	**1000**

Department	**Mathematics**	Programme**: M.Tech. – VLSI & ES**						
Semester	**I**	Course Category: **BS**				End Semester Exam Type**: TE**		
Course Code	**P23MAT102**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Applied Mathematics for VLSI**	2	2	-	3	40	60	100

Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Explain language of graphs and trees	K2
	CO2	Define and apply various algorithms in graph theory	K2
	CO3	Describe about Boolean algebra and Boolean functions	K3
	CO4	Apply mathematical skills to model optimization problems.	K3
	CO5	Apply graph algorithm and Boolean functions to solve real time problems	K3

UNIT-I	**Basics of Graph Theory**	**Periods: 12**
Graphs – Data structures for graphs – Subgraphs – Operations on Graphs Connectivity – Euler, Hamilton graph and its properties- Planar graphs- Networks and the maximum flow – Minimum cut theorem - Trees –Spanning trees – Rooted trees – Matrix representation of graphs		**CO1**
UNIT-II	**Graph Algorithm**	**Periods: 12**
Computer Representation of graphs – Basic graph algorithms – Minimal spanning tree algorithm – Kruskal and Prim's algorithm - Shortest path algorithms – Dijsktra's algorithm – DFS and BFS algorithms. Lattices as partially ordered sets, properties of Lattices. Lattices as Algebraic Systems, Sublattices		**CO2**
UNIT-III	**Boolean Algebra**	**Periods: 12**
Definitions and examples, Subalgebra, Direct Product and Homomorphism. Boolean Functions, Representation and Minimization of Boolean Functions, Design examples using Boolean Algebra		**CO3**
UNIT-IV	**Optimization Techniques**	**Periods: 12**
Linear Programming – Formulation of LPP – Graphical methods - Simplex method- Transportation problems- Assignment problems.		**CO4**
UNIT-V	**Instructional Activities**	**Periods: 12**
Applications of Boolean Functions - Practical applications of Basic graph algorithms, Transportation problems and Assignment problems		**CO5**

Lecture Periods: 60	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 60**

Reference Books

1. Tremblley. J.P and Manohar. R, "Discrete Mathematics Structures with Application to Computer Science", Mc Graw Hill Book Company, 2017
2. Narsingh Deo, "Graph Theory: With Application to Engineering and Computer Science", PHI, 2014.
3. Kanti Swarup, Man Mohan, P.K. Gupta, "Operations Research ", Sultan Chand & Sons, 2014
4. Edgar G. Goodaire & Michael M. Parameter, "Discrete Mathematics with Graph Theory", 3rd edition, Pearson Education, 2018.

Web References

1. http:// www.nptel.ac.in
2. http://www.personal.psu.edu/cxg286/Math485.pdf
3. http://poincare.matf.bg.ac.rs/~zarkom/Book_Shaums_BooleanAlgebraMendelson.pdf
4. https://lecturenotes.in/subject/2/applied-mathematics-1-m-1

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	-	2	-	-	1	-	-
2	2	-	-	2	-	-	1	-	-
3	2	-	-	2	-	-	1	-	-
4	2	-	-	2	-	-	1	-	-
5	2	-	-	2	2	-	1	-	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: M.Tech. - VLSI & ES						
Semester	I	Course Category: PC			End Semester Exam Type: TE			
Course Code	P23VET101	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	Electronic Design Automation Tools	3	0	0	3	40	60	100

Course Outcome	On completion of the course, the students will be able to		BT Mapping (Highest Level)
	CO1	Understand Functional design and verification models.	K3
	CO2	Synthesize circuits using HDL codes.	K3
	CO3	Design circuits, IC design flow using PSPICE tool,	K3
	CO4	Design Mixed signal design flow for integrated circuit design.	K3
	CO5	Implement Microelectronics design using Electronic Design Automation (EDA) tools.	K4

Unit-I	Simulation Using HDL	Periods: 9
Simulation-Types of Simulation, Logic Systems, Working of Logic Simulation, Cell Models, Delay Models, State Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation.		CO1
Unit-II	**Synthesis Using HDL**	**Periods: 9**
Verilog and Logic Synthesis, VHDL and Logic Synthesis, Memory Synthesis, FSM Synthesis, Memory Synthesis, Performance-Driven Synthesis. CAD Tools for Simulation and Synthesis: Modelsim and Leonardo Spectrum		CO2
Unit-III	**Circuit Design and Simulation Using PSPICE**	**Periods: 9**
Pspice Models for Transistors, A/D & D/A Sample and Hold Circuits etc., and Digital System Building Blocks, Design and Analysis of Analog and Digital Circuits Using PSPICE.		CO3
Unit-IV	**An Overview of Mixed Signal VLSI Design**	**Periods: 9**
Fundamentals of Analog and Digital Simulation, Mixed Signal Simulator Configurations, Understanding Modeling, Integration to CAD Environments.		CO4
Unit-V	**Instructional Activities**	**Periods: 9**
Simulation of delay models using digital logic circuits- FSM Synthesis- Simulation of Transistor amplifier circuit- Mixed signal simulation environment setup		CO5

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Books

1. J.Bhaskar, “A Verilog Primer”, BSP, 2003.
2. J.Bhaskar, “A Verilog HDL Synthesis”, BSP, 2003.
3. M.H.Rashid, “SPICE FOR Circuits and ElectronicsUsing PSPICE”, (2/E) (1992) Prentice Hall.
4. M.J.S.Smith, “Application-Specific Integrated Circuits”,(1997). Addison Wesley.

Web References

1. https://nptel.ac.in/courses/106105083
2. https://onlinecourses.swayam2.ac.in/aic20_sp59/preview
3. https://www.btechguru.com/courses--nptel----electronic-design-automation-video-lecture--cse--CS100413V.html
4. https://cosmolearning.org/courses/electronic-design-automation-544/

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	2	1	2	-	1	3	2	-
2	2	2	1	2	-	1	3	2	-
3	2	2	1	2	-	1	3	2	-
4	2	2	1	2	-	1	3	2	-
5	2	2	1	2	2	1	3	2	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: M.Tech. – VLSI & ES						
Semester	I	Course Category: PC			End Semester Exam Type: TE			
Course Code	P23VET102	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	FPGA Based System Design	3	0	0	3	40	60	100

Course Outcome	On completion of the course, the students will be able to	BT Mapping (Highest Level)
	CO1 Describe the various basic modules of FPGA	K2
	CO2 Relate the technology mapping with FPGA	K3
	CO3 Discuss the routing concepts of FPGA	K3
	CO4 Classify the various FPGA architectures	K4
	CO5 Synthesize various multipliers & filters	K4

Unit-I	FPGA Architecture	Periods: 9
Introduction of basic concepts, Digital design and FPGAs. FPGA based system design, Logic blocks, Routing architecture, FPGA Fabrics, Circuit design of FPGA fabrics, Platform FPGA		CO1
Unit-II	**Technology Mapping for FPGAs**	**Periods: 9**
Fundamental of high level synthesis, Logic synthesis, Logic optimization and technology mapping, Lookup table technology mapping, Timing analysis, Timing optimization, Area optimization		CO2
Unit-III	**Routing for FPGAs**	**Periods: 9**
Routing terminology, Strategy for routing in FPGAs, Routing for row-logic block selection, Experimental procedure Logic block architecture, Logic block functionality vs area and efficiency, Logic block selection, Experimental procedure, Logic block area and routing model		CO3
Unit-IV	**Architecture of FPGAs**	**Periods: 9**
Study of Xilinx Virtex series FPGAs, Architecture of Altera cyclone FPGA series. Comparison of Xilinx & Altera FPGAs		CO4
Unit-V	**Instructional Activities**	**Periods: 9**
Synthesis of multiplier and digital filters in FPGA and analyse the FPGA architecture and mapping of I/O pads		CO5

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Books

1. Wayne Wolf, FPGA based system design, Prentice Hall, 2004.
2. Wayne Wolf, Modern VLSI design, System on Chip design, 3rd Ed. Prentice Hall 2002.
3. S. Trimberger, Edr, Field Programmable Gate Array technology, Kluwer Academic publication, 2009
4. Pong P. Chu, "FPGA Prototyping by VHDL / Verilog Examples "Wiley Publisher, 2008

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1. http://nptel.iitm.ac.in
2. https://dl.acm.org/doi/book/10.5555/983326
3. https://www.academia.edu/31100712/FPGA-Based_System_Design_Wayne_Wolf_SAmple_book
4. https://trove.nla.gov.au/work/38674264

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	3	-
2	2	-	3	3	-	1	3	3	-
3	2	-	3	3	-	1	3	3	-
4	2	-	3	3	-	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: M.Tech. – VLSI & ES						
Semester	I	Course Category: PC			End Semester Exam Type: TE			
Course Code	P23VET103	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	VLSI Design Techniques	3	-	-	3	40	60	100

Course Outcome	On completion of the course, the students will be able to	BT Mapping (Highest Level)
	CO1 Demonstrate the characteristics of MOS transistors with its small signal parameters	K3
	CO2 Draw stick diagram and design circuits in static and dynamic CMOS logic	K3
	CO3 Estimate the VLSI circuit performance based on resistors, inductors and capacitors.	K3
	CO4 Design combinational and sequential circuits in VLSI and understand its clock distribution	K3
	CO5 Code the combinational and sequential circuits in Verilog HDL language	K4

Unit-I	**MOS Transistor Theory and Process Technology**	**Periods: 9**
NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology		**CO1**
Unit-II	**Inverters and Logic Gates**	**Periods: 9**
NMOS and CMOS Inverters, stick diagram, Inverter ratio, DC and transient characteristics, switching times, Super buffers, Driving large capacitance loads, CMOS logic structures, Transmission gates, Static CMOS design, dynamic CMOS design		**CO2**
Unit-III	**Circuit Characterization and Performance Estimation**	**Periods: 9**
Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing. Scaling		**CO3**
Unit-IV	**VLSI System Components, Circuits and Design**	**Periods: 9**
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing		**CO4**
Unit-V	**Instructional Activities**	**Periods: 9**
Case study on Overview of digital design with Verilog HDL for Structural, Data flow, Behavioral Styles of Hardware Description		**CO5**

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Books

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2. John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley &Sons, Inc., 2002.
3. Samir Palnitkar, “Verilog HDL”, Pearson Education, 2nd Edition, 2004
4. James D Plummer, Michael D. Deal, Peter B.Griffin, “Silicon VLSI Technology: fundamentals practice and Modeling”, Prentice Hall India, 2009

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1. http://web.ewu.edu
2. http://ic.sjtu.edu
3. http://nptel.iitm.ac.in

4. http://ee.ncu.edu.tw/~jfli/vlsi21/lecture/ch01.pdf

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	3	-
2	2	-	3	3	-	1	3	3	-
3	2	-	3	3	-	1	3	3	-
4	2	-	3	3	-	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech**. – **VLSI & ES**						
Semester	**I**	Course Category: **HS**			End Semester Exam Type: **TE**			
Course Code	**P23HSTC01**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Research Methodology and IPR**	3	0	0	3	40	60	100

Common to all the M.Tech (ECE and VLSI & ES)

Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
CO1	Formulate research problem	K2
CO2	Carry out research analysis	K2
CO3	Follow research ethics	K2
CO4	Describe today's world is controlled by Computer, Information Technology, but tomorrow world will beruled by ideas, concept, and creativity	K2
CO5	Interpret IPR and filing patents in R & D	K3

Unit-I	**Research Problem Formulation**	**Periods: 9**
Meaning of research problem- Sources of research problem, criteria characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations		**CO1**
Unit-II	**Literature Review**	**Periods: 9**
Effective literature studies approaches, analysis, plagiarism, and research ethics		**CO2**
Unit-III	**Technical writing / Presentation**	**Periods: 9**
Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal, a presentation and assessment by a review committee.		**CO3**
Unit-IV	**Introduction to Intellectual Property Rights (IPR)**	**Periods: 9**
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT		**CO4**
Unit-V	**Instructional Activities**	**Periods: 9**
Case study- Identification of research problems- Development of a resource proposal- Literature review- Analysis on Property rights infringement		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'" Kenwyn Publisher, 1996
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"2nd edition, Lansdowne publisher, 2001
3. C.R. Kothari, Gaurav Garg, New Age International, Research Methodology: Methods and Techniques 4th Edition, 2018
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd, 2007.

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2. https://www.isical.ac.in/~palash/research-methodology/RM-lec9.pdf

3. https://www.wipo.int/edocs/pubdocs/en/intproperty/958/wipo_pub_958_3.pdf
4. https://lecturenotes.in/m/21513-research-methodology-

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	3	2	1	1	2	1	1	-	-
2	3	2	1	1	2	1	1	-	-
3	3	2	1	1	2	1	1	-	-
4	3	2	1	1	2	1	1	-	-
5	3	2	1	1	2	1	1	-	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme**: M.Tech. – VLSI & ES**						
Semester	**I**	Course Category: **PC**			End Semester Exam Type: **LE**			
Course Code	**P23VEP101**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**VLSI Design Laboratory**	0	0	4	2	50	50	100

			BT Level
Course Outcome	**On completion of the course, the students will be able to**		
	CO1	Design and simulate combinational circuits in Verilog HDL	K4
	CO2	Design and simulate sequential circuits in Verilog HDL	K4
	CO3	Design and simulate VLSI circuits using spice tool	K4
	CO4	Interface FPGA with PC for I/O interfacing	K5
	CO5	Implement combinational and sequential circuits using FPGA/CPLD	K5

List of Lab Experiments

1. Design and simulate combinational circuits using VHDL/Verilog HDL in Gate level, behavior level and generate test vectors
   - Adder, subtractor
   - Code converter
   - Decoder
   - Encoder
   - Multiplexer
   - Demultiplexer
   - Multiplier
   - Divider
2. Design and simulate sequential circuits using VHDL/Verilog HDL in Gate level, behavior level and generate test vectors
   - Flip-flops
   - Shift registers (SISO, SIPO, PISO, PIPO)
   - Synchronous counter
   - Asynchronous counter
   - Mod counter
   - Sequence generator
   - Sequence detector
   - Ring and Johnson counter
3. Simulation of NMOS and CMOS circuits using SPICE.
4. FPGA/CPLD real time programming and I/O interfacing.
5. Implementation of combinational circuit in FPGA/CPLD
6. Implementation of sequential circuit in FPGA/CPLD

Reference Books:

1. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, “Digital Integrated Circuits - A Design Perspective “, Prentice Hall of India, 2012.
2. James D Plummer, Michael D. Deal, Peter B.Griffin, “Silicon VLSI Technology: fundamentals practice and Modeling”, Prentice Hall India, 2009.
3. Thomas, D. E., Philip.R. Moorby “The Verilog Hardware Description Language”,2nd edition, Kluwer Academic Publishers,2002.
4. DebaPrasad Das, VLSI Design”, Oxford University Press, 2012.

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2. http://nptel.iitm.ac.in
3. http://ee.ncu.edu.tw/~jfli/vlsi21/lecture/ch01.pdf
4. https://www.tutorialspoint.com/vlsi_design/vlsi_design_digital_system.htm

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	1	3	1	-	1	3	3	-
CO2	2	1	3	1	-	1	3	3	-
CO3	2	1	3	1	-	1	3	3	-
CO4	2	1	3	1	-	1	3	3	-
CO5	2	1	3	1	-	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	Performance in practical classes			Model Practical Examination	Attendance		
	Conduction of practical	Record work	viva				
Marks	15	5	5	15	10	50	100

Department	**Electronics and Communication Engineering**	Programme**: M.Tech. – VLSI & ES**						
Semester	**I**	Course Category: **HS**				End Semester Exam Type**: LE**		
Course Code	**P23HSPC01**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Technical Seminar and Report Writing**	0	0	4	2	50	50	100

Common to all the M.Tech (ECE and VLSI & ES)

		On completion of the course, the students will be able to	**BT Level**
Course Outcome	**CO1**	Select a subject, narrowing the subject into a topic	2
	CO2	Explain objective and collect the relevant bibliography	2
	CO3	Describe the papers and understand the author's contributions and critically analyzing each paper	3
	CO4	Prepare a working outline and linking the papers and preparing a draft of the paper	2
	CO5	Prepare conclusions based on the reading of all the papers, Writing the Final Paper, and giving final Presentation	3

Activity	**Instructions**	**Submission week**	**Evaluation**
Selection of area of interest and Topic	select an area of interest, topic and state an objective	2nd week	**3 %** Based on clarity of thought, current relevance and clarity in writing
Stating an Objective			
Collecting Information about area & topic	• List 1 Special Interest Groups or professional society • List 2 journals • List 2 conferences, symposia or workshops • List 1 thesis title • List 3 web presences (mailing lists, forums, news sites) • List 3 authors who publish regularly in your area • Attach a call for papers (CFP) from your area.	3rd week	**3%** (The selected information must be area specific and of international and national standard)
Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter	• Provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar • When picking papers to read - try to: - Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them. - Favour papers from well-known journals and conferences, in the field (as indicated in other Favour more recent papers, - Pick a recent survey of the field so you can quickly gain an overview, Find relationships with respect to each other and to your topic area (classification scheme/categorization) - Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered	4th week	6% (The list of standard papers and reason for selection)

Reading and notes for first 5 papers	Reading Paper Process For each paper form a Table answering the following questions: • What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • What simplifying assumptions does the author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? • Conclude with limitations/issues not addressed by the paper (from the perspective of survey)	6th week	8% (The table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for next 5 papers	Repeat Reading Paper Process	7th week	8% (The table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper
Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	8% (This component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	6% (Clarity, purpose and conclusion) 6% Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	5% (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11th week	10% (this component will be evaluated based on the linking and classification among the papers)
Conclusions	Write your conclusions and future work	12th week	5% (conclusions)
Final Draft	Complete the final draft of your paper	13th week	10% (formatting, English, Clarity and linking) 4% Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th & 15th week	10% (based on presentation and Viva-voce)

* TE – Theory Exam, LE – Lab Exam

COs/ POs/ PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	3	3	1	3	3	3	-	-

2	2	3	2	1	3	2	3	-	-
3	2	3	2	1	3	2	3	-	-
4	2	3	2	1	3	2	3	-	-
5	2	3	2	1	3	2	3	-	-

Correlation Level: 1-Low, 2-Medium, 3-High

Evaluation Method

Assessment	**Continuous Assessment Marks (CAM)**				**Attendance**	**End Semester Examination (ESE) Marks**	**Total Marks**
	Weekly Progress	**Seminar**	**Record work**	**Viva**			
Marks	40	30	10	10	10	-	100

PROFESSIONAL ELECTIVE COURSES		
Professional Elective–I (Offered in Semester I)		
Sl. No	**Course Code**	**Course Title**
1	P23VEE101	Principles of ASIC Design
2	P23VEE102	VLSI Architecture
3	P23VEE103	Physical Design of VLSI
4	P23VEE104	Real-Time Systems
5	P23VEE105	Analog IC Design

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. - VLSI & ES**						
Semester	**I**	Course Category Code: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE101**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Principles of ASIC Design**	3	0	0	3	40	60	100

Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Demonstrate VLSI tool-flow and appreciate FPGA architecture.	K2
	CO2	Describe the concepts of ASIC design methodology, data path elements, operators, I/O cells.	K3
	CO3	Write the Verilog/VHDL coding of VLSI circuit and generate automatic test pattern.	K3
	CO4	Explain algorithms for floor planning and placement of cells for optimized area and speed.	K3
	CO5	Illustrate the Spartan 3E, Xilinx, Vertex FPGA devices and its specifications, I/O blocks.	K4

Unit - I	**Introduction To Programmable Devices**	**Periods: 9**
Programmable logic devices: ROM - PLA - PAL - PLD - FPGA - features, programming and applications usingcomplex programmable logic devices; Speed performance and system programmability.		**CO1**
Unit - II	**Introduction To ASIC**	**Periods: 9**
Design flow - types of ASICs - full custom with ASIC - semi custom ASICs - standard cell based ASIC - gate array based ASIC - channeled – channel less - structured - data path elements - adders - multiplier - cell compilers ; Logical effort : area and efficiency - paths - multi stage cells - optimum delay.		**CO2**
Unit - III	**Low Level Design Language**	**Periods: 9**
EDIF: PLA tools - introduction to CFI designs representation; Half gate ASIC: Introduction to synthesis and simulation - two level logic synthesis - high level logic synthesis - VHDL and logic synthesis - types of simulation - boundary scan test - fault simulation - automatic test pattern generation.		**CO3**
Unit - IV	**Floor Planning, Placement And Routing**	**Periods: 9**
Physical design: CAD tools - system partitioning - estimating ASIC size - partitioning methods; Floor planning tools - I/O and power planning - clock planning - placement algorithms - iterative placement improvement; Time driven placement methods - physical design flow global routing - local routing - detail routing - special routing - circuit extraction and DRC.		**CO4**
Unit - V	**Instructional Activities**	**Periods: 9**
Synthesis of Spartan 3E and Vertex Board Analysis - inputs and outputs - clock and power inputs - Xilinx I/O blocks - PLAs and PALs design using ASIC board.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Smith M J S, “Application Specific Integrated Circuits”, Pearson Education, 2009.
2. Farzad N, Faranak N, “From ASICs to SOCs: A practical Approach”, Prentice Hall, 2003.
3. Wayne Wolf, "FPGA-Based System Design", Prentice Hall, 2004.
4. Farzad N, “Timing Verification of Application Specific Integrated Circuits”, 3rd Edition, Prentice Hall, 2004.

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sign_Techniques www.utdallas.edu/~zhoud/DesignEntry.
2. en.wikipedia.org/wiki/High-level_synthesis.
3. https://www.electronics-notes.com/articles/digital-embedded-processing/asic-application-specific-ic/how- to-design-asic.php.
4. https://www.engr.siu.edu/haibo/ece428/notes/ece428_intro

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	3	-
2	2	-	3	3	-	1	3	3	-
3	2	-	3	3	-	1	3	3	-
4	2	-	3	3	-	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: **M.Tech. - VLSI & ES**						
Semester	I	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	P23VEE102	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**VLSI Architecture**	3	0	0	3	40	60	100

Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Recognizes the various static and dynamic circuit design concepts.	**K2**
	CO2 Outline the different programmable logic devices with its application.	**K3**
	CO3 Solve the algorithms for various compaction terminologies.	**K3**
	CO4 Build the digital circuits with analog VLSI design.	**K3**
	CO5 Design the various digital circuits using HDL.	**K4**

Unit - I	**CMOS Design**	**Periods: 9**
Overview of digital VLSI design Methodologies- Logic design with CMOS-transmission gate circuits-Clocked CMOS-dynamic CMOS circuits, Bi-CMOS circuits- Layout diagram, Stick diagram-IC fabrications – Trends in IC technology.		**CO1**
Unit - II	**Programmable Logic Devices**	**Periods: 9**
Programming Techniques-Anti fuse-SRAM-EPROM and EEPROM technology – Re Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects, XilinxXC9500, Cool Runner - XC-4000, XC5200, SPARTAN, Virtex - Altera MAX 7000-Flex 10KStratix.		**CO2**
Unit - III	**Basic Construction, Floor Planning, Placement And Routing**	**Periods: 9**
System partition – FPGA partitioning – Partitioning methods- floor planning – placement physical design flow – global routing – detailed routing – special routing- circuit extraction – DRC.		**CO3**
Unit - IV	**Analog VLSI Design**	**Periods: 9**
Introduction to analog VLSI- Design of CMOS 2-stage – 3-stage Op-Amp –High Speed and High frequency op-amps-Super MOS-Analog primitive cells-realization of neural networks		**CO4**
Unit - V	**Instructional Activities**	**Periods: 9**
Synthesis of the Ripple Carry Adder, Multiplier, Comparator, Shift registers and ALU circuits in CPLD devicesand analyze the design with architecture.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Wayne Wolf, “Modern VLSI design “Prentice Hall India,2006.
2. Samir Palnitkar, “Verilog HDL, A Design guide to Digital and Synthesis” 2nd Edition, Pearson,2005.
3. John P. Uyemera “Chip design for submicron VLSI cmos layout and simulation “, Cengage Learning India Edition”, 2011.
4. Natarajan Saravana Kumar, Krishnasamy Natarajan Vijeyakumar and Karuppanan Sakthisudhan, “VLSI Architectures “, LAP Lambert Academic Publishing, 2016

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3. https://www.tutorialspoint.com/digital_circuits
4. http://www.vlsisystemdesign.com.html

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	3	-
2	2	-	3	3	-	1	3	3	-
3	2	-	3	3	-	1	3	3	-
4	2	-	3	3	-	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. - VLSI & ES**						
Semester	**I**	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE103**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Physical Design of VLSI**	3	0	0	3	40	60	100

Course Outcome		**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1	Explain the concepts of VLSI technology in physical design.	**K3**
	CO2	Illustrate the concept of Placement using various algorithms.	**K3**
	CO3	Illustrate the Routing methodologies using various algorithms.	**K4**
	CO4	Conclude the concepts of delay modeling& delay minimization	**K4**
	CO5	Examine single layer and over the cell routing and apply 1D and 2D compaction techniques.	**K3**

Unit - I	**Introduction to VLSI Technology**	**Periods: 9**
Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein- Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array (FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms.		**CO1**
Unit - II	**Placement Using Top-Down Approach**	**Periods: 9**
Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic- Ratio-cut- partition with capacity and i/o constraints; Floor planning: Rectangular dual floor planning- hierarchical approach-simulated annealing- Floor plan sizing; Placement: Cost function- force directed method- placement by simulated annealing- partitioning placement- module placement on a resistive network – regular placement- linear placement		**CO2**
Unit - III	**Routing Using Top Down Approach**	**Periods: 9**
Fundamentals: Maze running- line searching- Steiner trees; Global Routing: Sequential Approaches-hierarchical approaches- multi-commodity flow based techniques- Randomised Routing- One Step approach- Integer Linear Programming; Detailed Routing: Channel Routing- Switch box routing; Routing in FPGA: Array based FPGA- Row based FPGAs		**CO3**
Unit - IV	**Performance Issues in Circuit Layout**	**Periods: 9**
Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization- unconstrained via Minimization- Other issues in minimization		**CO4**
Unit - V	**Instructional Activities**	**Periods: 9**
Design Layouts for basic combinational circuits- Floor planning using Annealing- Routing algorithm for channel routing in FPGA- Implementation of gate delay models to estimate delays in RC trees		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Sung Kyu Lim, “Practical Problems in VLSI Physical Design Automation”, Springer-Verlag New York Inc.,2008
2. Ban Wong, Anurag Mittal Yu Cao and Greg Starr, “Nano CMOS Circuit and Physical Design” Wiley, 2004
3. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer Academic, 2002
4. Krishna Lal Baishnab and Kiran Maiye, “Convex Optimisation on Routing in VLSI Physical Design”, LAP Lambert Academic Publishing, 2017

Web References

1. http://www2.inf.uos.de/papers_html/
2. http://ic.sjtu.edu
3. https://www.ifte.de/books/eda/chap1.pdf
4. https://nptel.ac.in/courses/106/105/106105161/

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	3	-
2	2	-	3	3	-	1	3	3	-
3	2	-	3	3	-	1	3	3	-
4	2	-	3	3	-	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Dr. P. Raja, Chairman - Bos

Department	Electronics and Communication Engineering	Programme: **M.Tech. - VLSI & ES**						
Semester	I	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	P23VEE104	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Real Time Systems**	3	0	0	3	40	60	100

			BT Mapping (Highest Level)
Course Outcome	**On completion of the course, the students will be able to**		
	CO1	Distinguish Real time operating systems and operating system.	**K3**
	CO2	Describe multitask scheduling involved in real time systems.	**K3**
	CO3	Explain the programming language and tools.	**K3**
	CO4	Illustrate the concepts on real time Databases.	**K3**
	CO5	Illustrate the characteristics of real time systems.	**K3**

Unit - I	**Introduction**	**Periods: 9**
Introduction – Issues in Real Time Computing – Structure of a Real Time System – Task classes Performance Measures for Real Time Systems – Estimating Program Run Times – Characteristics of Real-time Systems – Classification of Real-time systems – Applications of Real-time Systems – Safety and Reliability. Basic Concepts of Scheduling: Real-time applications - Basic concepts for real-time task scheduling. Scheduling of Independent Tasks: Basic on-line algorithms for periodic tasks - Hybrid task sets scheduling.		**CO1**
Unit - II	**Scheduling in Real-Time Systems**	**Periods: 9**
Scheduling of Dependent Tasks: Tasks with precedence relationships - Tasks sharing critical resources. Scheduling schemes for handling overload: Scheduling techniques in overload conditions - Handling real-time tasks with varying timing parameters - Handling overload conditions for hybrid task sets. Multiprocessor scheduling and comparison with uniprocessor scheduling		**CO2**
Unit - III	**Programming Language and Tools**	**Periods: 9**
Programming Languages and Tools – Desired language characteristics – Data typing – Control structures Facilitating Hierarchical Decomposition, Packages, Run time (Exception) Error handling – Overloading and Generics – Multitasking – Low level programming – Task Scheduling – Timing Specifications		**CO3**
Unit - IV	**Real Time Databases**	**Periods: 9**
Real time Databases – Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two – phase Approach to improve Predictability – Maintaining Serialization Consistency – Databases for Hard Real Time Systems.		**CO4**
Unit - V	**Instructional Activities**	**Periods: 9**
Simulation of Task scheduling and Management-Real Time Database system-Case study		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Stuart Bennett, “Real-time Computer Control”, Second Edition, Pearson Education Ltd., 2012.
2. Francis Cottet, Joelle Delacroix and ZoubirMammeri, “Scheduling in Real-Time Systems”, John Wiley &Sons Ltd., 2002.
3. Liu, Jane W. S.Real-time systems Upper Saddle River, N.J.: Prentice Hall, cop. 2000.
4. Mall Rajib, “Real Time Systems”, Pearson Education, 2009

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1. nptel.ac.in/courses/106105036
2. http://www.slideshare.net/sanjivmalik/rtos-concepts

3. http://class.ece.iastate.edu/cpre458/lecture_notes.htm
4. http://www.eecs.umich.edu/courses/eecs571/lectures/lecture1-intro

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	1	1	3	-	3
2	2	-	3	3	1	1	3	-	3
3	2	-	3	3	1	1	3	-	3
4	2	-	3	3	1	1	3	-	3
5	2	2	3	3	2	1	3	-	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. - VLSI & ES**						
Semester	**I**	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE105**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Analog IC Design**	3	0	0	3	40	60	100

Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Design amplifiers to meet user specifications	**K3**
	CO2	Analyze the frequency and noise performance of amplifiers	**K4**
	CO3	Design and analyze feedback amplifiers and one stage op amps	**K4**
	CO4	Design and analyze two stage op amps	**K4**
	CO5	Design and analyze current mirrors and current sinks with MOS devices	**K4**

UNIT- I	**Single Stage Amplifiers**	**Periods: 9**
Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, designof Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.		**CO1**
UNIT- II	**High Frequency and Noise Characteristics of Amplifiers**	**Periods: 9**
Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.		**CO2**
UNIT- III	**Feedback and Single Stage Operational Amplifiers**	**Periods: 9**
Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.		**CO3**
UNIT- IV	**Stability and Frequency Compensation of Two Stage Amplifier**	**Periods: 9**
Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage And Using Cascode Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, And Compensation Of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.		**CO4**
UNIT- V	**Instructional Activities**	**Periods: 9**
Small-Signal Analysis of MOSFET Amplifiers- Design of Op amps with Feedback configurations- Implementation of Frequency compensation of Two-stage Amplifiers		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Jacob Baker “CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3rdEdition, 2010.
2. Willey M.C. Sansen, “Analog Design Essentials”, Springer, 2006.
3. Grebene, “Bipolar and Mos Analog Integrated Circuit Design”, John Wiley & Sons, Inc.,2003.
4. Phillip E.Allen, Douglas R .Holberg, “Cmos Analog Circuit Design”, Oxford University Press, 2ndEdition, 2002.

Web References

1. https://archive.nptel.ac.in/courses/117/106/117106030/
2. https://onlinecourses.nptel.ac.in/noc22_ee15/preview
3. https://onlinecourses.nptel.ac.in/noc22_ee34/preview
4. https://www.udemy.com/topic/analog-circuits/

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	-	2	-	-	1	-	-
2	2	-	-	2	-	-	1	-	-
3	2	-	-	2	-	-	1	-	-
4	2	-	-	2	-	-	1	-	-
5	2	-	-	2	2	-	1	-	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

SEMESTER – II

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23VETC01	Advanced Digital System Design	PC	3	0	0	3	40	60	100
2	P23VETC02	Embedded Processors	PC	3	0	0	3	40	60	100
3	P23VETC03	Embedded System Design	PC	3	0	0	3	40	60	100
4	P23VET204	Low Power Digital VLSI Design	PC	3	0	0	3	40	60	100
5	P23VEE2XX	Professional Elective-II	PE	3	0	0	3	40	60	100
6	P23VEE2XX	Professional Elective-III	PE	3	0	0	3	40	60	100
Practical										
7	P23VEP202	Embedded System Design Laboratory	PC	0	0	4	2	50	50	100
8	P23HSPC02	Seminar on ICT a hands-on approach	HS	0	0	4	2	100	-	100
Employability Enhancement Course										
9	P23ECC2XX	Certification Course – II	AEC	0	0	4	-	100	-	100
10	P23ACT20X	Audit Course - II	AEC	2	0	0	-	100	-	100
Total							**22**	**590**	**410**	**1000**

Department	Electronics and Communication Engineering				Programme: **M.Tech. – VLSI & ES**			
Semester	**II**				Course Category: **PC**		End Semester Exam Type: **TE**	
Course Code	**P23VETC01**				Periods/Week		Credit	Maximum Marks
					L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Advanced Digital System Design**				3	-	-	3	40	60	100
Common to all the M.Tech (ECE and VLSI & ES)											
Course Outcome	**On completion of the course, the students will be able to**										BT Mapping (Highest Level)
	CO1	Realize the Algorithmic State Machine									**K3**
	CO2	Design and analyze the asynchronous sequential digital circuits									**K3**
	CO3	Design and analyze the synchronous sequential circuits using PLDs									**K3**
	CO4	Identify the fault in the digital circuits									**K3**
	CO5	Simulate and synthesis the sequential circuits									**K4**

Unit-I	**Sequential Circuit Design**	**Periods: 9**
Analysis of clocked synchronous sequential circuits and modeling- state diagram - state table - state table assignment and reduction - design of iterative circuits - ASM chart and realization using ASM		**CO1**
Unit-II	**Asynchronous Sequential Circuit Design**	**Periods: 9**
Analysis of asynchronous sequential circuit: Design of asynchronous sequential circuit - static and dynamic methods - flow table reduction - races - state assignment transition table and problems in transition table - essential hazards - data synchronizers - mixed operating mode asynchronous circuits		**CO2**
Unit-III	**Synchronous Design Using Programmable Devices**	**Periods: 9**
Programming logic device families: Designing a synchronous sequential circuit using PLA/PAL - realization of finite state machine using PLD/FPGA		**CO3**
Unit-IV	**Fault Diagnosis and Testability Algorithms**	**Periods: 9**
Fault diagnosis method: Path sensitization method - Boolean difference method - D – algorithm - tolerance techniques - compact algorithm - fault in PLA/PAL- test generation - DFT schemes - built in self-test		**CO4**
Unit-V	**Instructional Activities**	**Periods: 9**
Simulation of synchronous/ asynchronous sequential circuits: Logic compilation - two level and multi-level logic synthesis - sequential logic synthesis -technology mapping - tools for mapping to PLDs and FPGAs		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Charles H R Jr, Larry L K, “Fundamentals of Logic Design “, 7th Edition, Global Engineering, 2014.
2. Parag K L, ‘Fault Tolerant and Fault Testable Hardware Design” 1st Edition, B S Publications, 2002.
3. ParagK.L, “Digital system Design using PLD “, B S Publications,2003
4. Stephen Brown, and Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design", Third Edition, McGraw-Hill, 2014.

Web References

1. http://nptel.ac.in/courses/117108040/downloads/Digital%20System%20Design.pdf
2. https://www.doulos.com/knowhow/verilog_designers_guide/
3. https://lecturenotes.in/notes/15423-note-for-digital-system-design-dsd-by-vtu-rangers
4. https://www.sjsu.edu/people/thuy.le/docs/271syl.pdf

***** TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	3	-
2	2	-	3	3	-	1	3	3	-
3	2	-	3	3	-	1	3	3	-
4	2	-	3	3	-	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

Department	**Electronics and Communication Engineering**	Programme**: M.Tech.- VLSI & ES**						
Semester	**II**	Course Category: **PC**			End Semester Exam Type**: TE**			
Course Code	**P23VETC02**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Embedded Processors**	3	0	0	3	40	60	100

Common to all the M.Tech (ECE and VLSI & ES)

Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Analyze the architectures of different Embedded Processors	3
	CO2 Identify an appropriate on chip peripherals for serial and parallel communication	2
	CO3 Examine the functions of ARM processors	3
	CO4 Develop real time applications using ARM processors	3
	CO5 Develop a firmware for embedded applications	3

Unit-I	**Introduction to Embedded Processors**	**Periods: 9**
Introduction to embedded processors– Compare Von Neumann architecture and Harvard architecture, RISC Vs CISC – System on Chip (SoC)-Introduction to SoC Architecture, An approach for SOC Design, System Architecture and Complexity. Processor Selection for SOC, Basic concepts in Processor Architecture, Overview of SOC external memory, Internal Memory, Scratchpads and Cache memory, SOC Memory System, Models of Simple Processor – memory interaction, SOC Standard Buses		**CO1**
Unit-II	**Embedded Processors on Chip Peripherals**	**Periods: 9**
Memory - Interrupts - I/O Ports-Timers & Real Time Clock (RTC), Watch dog timer - CCP modules - Capture Mode - Compare Mode-PWM Mode - Serial communication module - USART - SPI interface - I2C interface, Analog Comparator, Analog interfacing and data acquisition.		**CO2**
Unit-III	**ARM Processor**	**Periods: 9**
Architecture of ARM Controller – Registers, Pipeline organization 3 stage & 5 stage, Thumb mode of operation - D/A and A/D converter, sensors, actuators and their interfacing – Case study- Digital clock, Temperature sensing, Light sensing, Introduction to Internet of Things, smart home concepts		**CO3**
Unit-IV	**Real World Interfacing Using ARM Processor**	**Periods: 9**
Interfacing the peripherals to LPC2148: GSM and GPS using UART, on-chip ADC using interrupt (VIC), EEPROM using I2C, SD card interface using SPI, on-chip DAC for waveform generation.		**CO4**
Unit-V	**Instructional Activities**	**Periods: 9**
ARM CORTEX series embedded system design: CORTEX A, CORTEX M, CORTEX R processors series and versions for complex applications in embedded system, Firmware development for ARM Cortex, CORTEX M3 based controllers.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. F. Vahid and T. Givargis, “Embedded System Design: A Unified Hardware/Software Introduction”, Wiley India Pvt. Ltd., 2002.
2. Lyla B. Das, “Architecture, Programming and Interfacing of Low-power Processors ARM 7, Cortex-M”, Cengage, 1st Edition, 2017.
3. Embedded Systems: Real-Time Interfacing to ARM Cortex-M Microcontrollers,2014, Jonathan W Valvano CreateSpace publications ISBN: 978-1463590154.
4. Andrew Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s Guide – Designing and Optimizing System Software”, ELSEVIER

Web References

1. LPC 214x User manual (UM10139): - www.nxp.com
2. LPC 17xx User manual (UM10360): - www.nxp.com
3. http://processors.wiki.ti.com/index.php/HandsOn_Training_for_TI_Embedded_Processors
4. http://processors.wiki.ti.com/index.php/MCU_Day_Internet_of_Things_2013_Workshop

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	3	3	3	3	3	-	3	2	-
2	3	3	3	3	3	-	3	2	-
3	3	3	3	3	3	-	3	2	-
4	3	3	3	3	3	-	3	2	-
5	3	3	3	3	3	-	3	2	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

Department	**Electronics and Communication Engineering**	Programme**: M.Tech. – VLSI & ES**						
Semester	**II**	Course Category: **PC**			End Semester Exam Type**: TE**			
Course Code	**P23VETC03**	**Periods/Week**			**Credit**	**Maximum Marks**		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Embedded System Design**	3	0	0	3	40	60	100

Common to all the M.Tech (ECE and VLSI & ES)

Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Analyze various architectures	K2
	CO2 Discuss about the performance evaluation of OS	K3
	CO3 Discuss about scheduling	K3
	CO4 Evaluate RTOS	K4
	CO5 Analyze on digital camera architecture	K4

Unit-I	**Introduction to Embedded Systems**	**Periods: 9**
Introduction to Embedded systems – Embedded hardware, Embedded software, Classification and Examples of embedded systems, System on Chip, Design process. Skills required for an embedded system designer. Overview of 8051 Architecture, Real world Interfacing, Introduction to advanced architectures – x86, ARM and SHARC architectures - Processor and Memory organization, Instruction level parallelism, Performance metrics, Processor and Memory selection.		**CO1**
Unit-II	**Program Design and Analysis**	**Periods: 9**
Formalism for system design using UML (Unified Modelling Language), Model for Program flow graph (flow graphs). Basic Compilation techniques, Optimization of execution time, program size, energy and power. Processes and Operating system: Multiple tasks and processes, context switching, OS states, structure, timing requirements, Scheduling policies, and Inter- process communication Mechanisms. Performance Evaluation of OS		**CO2**
Unit-III	**Real Time Scheduling**	**Periods: 9**
State-machines, State charts, traditional logics and real-time logic. Deterministic scheduling: assumptions and candidate Algorithms, RM (rate monotonic) and EDF (earliest deadline first),realizing the assumptions, priority inversion and inheritance, Execution time prediction: Approaches and issues, measurement of S/W by S/W, program analysis by timing scheme, prediction by optimization, system interferences and architectural complexities		**CO3**
Unit-IV	**Real Time Operating Systems**	**Periods: 9**
OS services, Process management, timer and event functions, Memory management, Device, file and I/O management, Interrupt Routines in RTOS environment, basic design using RTOS, Performance metrics, OS security issues, Comparative study of sample of RTOS such as eCOS, real time Linux, Windows CE.		**CO4**
Unit-V	**Instructional Activities**	**Periods: 9**
Case studies: Digital Camera hardware and software architecture, Mobile phone software for key inputs.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Wayne Wolf, “Computers as Components: Principles of Embedded Computing system Design,” 2nd Edition, Morgan Kaufmann Publishers, 2008.
2. Steve Furber, “ARM System-on-Chip Architecture”, 2nd Edition, Pearson Education, 2001

3. Raj Kamal, “Embedded Systems-Architecture, Programming and Design,” The McGraw Hill Companies, 2nd Edition, 2008.
4. Andrew N Sloss, Dominic Symes, Chris Wright, “ARM System Developer's Guide - Designing and Optimizing System Software”, 2006, Elsevier.

Web References

1. https://nptel.ac.in/courses/108/102/108102045/
2. https://nptel.ac.in/courses/106/105/106105193/
3. https://nptel.ac.in/courses/106/105/106105159/
4. http://www.nptelvideos.in/2012/11/embedded-systems.html

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	1	-	1	1	-	-	1	-	3
2	1	-	1	1	-	-	1	-	3
3	1	-	1	1	-	-	1	-	3
4	1	-	1	1	-	-	1	-	3
5	1	-	1	1	3	-	1	3	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

Department	Electronics and Communication Engineering	Programme: M.Tech. – VLSI & ES						
Semester	II	Course Category: PC			End Semester Exam Type: TE			
Course Code	P23VET204	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	Low Power Digital VLSI Design	3	-	-	3	40	60	100

Course Outcome	On completion of the course, the students will be able to	BT Mapping (Highest Level)
	CO1 Illustrate the type of power dissipation occurring in VLSI circuits.	K3
	CO2 Analyze the power dissipation in VLSI circuits.	K4
	CO3 Design and simulate VLSI circuits by different gate sizing and signal gating parameter.	K4
	CO4 Classify and design the type of energy recovery model needed for the VLSI circuit.	K4
	CO5 Simulate and analyze the power dissipation in SRAM and DRAM memories.	K4

Unit-I	**Power Dissipation**	**Periods: 9**
Introduction: Need for low power circuit design - sources of power consumption -design methodology - low power figure of merits - limits and applications of low power VLSI Design		**CO1**
Unit-II	**Power Analysis**	**Periods: 9**
Power Analysis: SPICE circuit simulation - discrete transistor modeling and analysis - gate level 0 logic simulation - architecture level analysis - data correlation analysis; Probabilistic Power Analysis: Random logic signals - probabilistic power analysis techniques - signal entropy		**CO2**
Unit-III	**Circuit AND Logic Level**	**Periods: 9**
Circuit Level: Transistor and gate sizing - equivalent pin ordering - network restructuring and reorganization - special latches and flip flops; Logic Level: Gate reorganization - signal gating - logic encoding - precomputation logic		**CO3**
Unit-IV	**Energy Recovery Techniques**	**Periods: 9**
Energy Recovery Techniques: Energy dissipation using the RC model - energy recovery circuit design - power reduction in clock networks - low power bus - delay balancing		**CO4**
Unit-V	**Instructional Activities**	**Periods: 9**
Simulation of Sources of power dissipation in SRAMs - Low power SRAM circuit techniques; Sources of power dissipation in DRAMs - Low power DRAM circuit techniques using related tools		**CO5**

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Books

1. Kaushik R and Sharat C P, “Low-Power CMOS VLSI Circuit Design”, Wiley Student Edition, 2009.
2. Gary K Y, “Practical Low Power Digital VLSI Design “, Kluwer Academic Publishers, 1998.
3. Bellaouar A and Elmasry M, “Low-Power Digital VLSI Design: Circuits and Systems”, Kluwer Academic Publishers, 1995
4. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits – Analysis and Design”, TMH, 2011.

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1. http://www.eeherald.com/section/design-guide/Low-Power-VLSI-Design.html
2. https://nptel.ac.in/courses/106/105/106105034/
3. https://lecturenotes.in/m/30442-low-power-digital-vlsi-design
4. https://www.egr.msu.edu/classes/ece410/salem/files/s16/lectures/Ch2_S2_N

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	3	-
2	2	-	3	3	-	1	3	3	-
3	2	-	3	3	-	1	3	3	-
4	2	-	3	3	-	1	3	3	-
5	2	2	3	3	3	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

Department	**Electronics and Communication Engineering**	Programme**: M.Tech. – VLSI & ES**						
Semester	**II**	Course Category: **PC**			End Semester Exam Type: **LE**			
Course Code	**P23VEP202**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Embedded System Design Laboratory**	0	0	4	2	50	50	100

Course Outcome	**On completion of the course, the students will be able to**		**BT** Level
	CO1	Interface a microcontroller to PC for communication	K3
	CO2	Interface various sensors using PIC and Arduino microcontrollers	K3
	CO3	Design various microcontroller-based systems	K3
	CO4	Communicate wirelessly using microcontroller	K3
	CO5	Process an image using Raspberry pi	K4

Lab Experiments

1. Interfacing the microcontroller to a PC through RS232 and displaying the messages sent by the microcontroller on the PC.
2. Design with PIC and Arduino Microcontrollers - Assembly or C Programming/Arduino IDE programming to interface
   - 7 segment displays to display the measured voltage from 0 to 5 volts
   - LDR and display light intensity in 7 segment display
   - Temperature sensor and display temperature in 7 segment display
   - Pressure sensor and display measured pressure in 7 segment display
   - PH sensor and display measured value in 7 segment display
   - Ultrasonic sensor and display distance in 7 segment display
   - Noise sensor and display noise level in 7 segment display
3. Interface DC motor with Microcontroller and control its speed and direction using PWM
4. Microcontroller based system design
   - Lamp controller using a light sensor and a timer
   - Water Pump Controller to maintain water level in a tank
   - Moisture controller using moisture and sprinkler controller
5. Design Real time clock
6. Wireless data transfer using Microcontroller
7. Color identification and tracking using Raspberry pi

Reference Books

1. Elaf A. Saeed, “Basics Labs for Embedded Systems Using Arduino: Arduino based projects”, LAP Lambert Academic Publishing, 2020
2. Tim Wilmshurst, “Designing Embedded Systems with PIC Microcontrollers: Principles and Applications”, Elsevier Science & Technology, 2011
3. Rajkamal, ‘Embedded System”, Tata McGraw Hill, 2003
4. Rettberg, A.; Zanella, M.; Domer, R.; Gerstlauer, A.; Rammig, F.Embedded System Design: Topics, Techniques and Trends, Springer, 2007.

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1. http://embedded-lab.com/
2. https://www.electronics-lab.com/embedded-systems-online-training-resources/
3. https://lecturenotes.in/subject/557/embedded-system-design-esd
4. https://users.ece.cmu.edu/~koopman/lectures/index.html

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	1	3	3	3	1	3	-	3
CO2	2	1	3	3	3	1	3	-	3
CO3	2	1	3	3	3	1	3	-	3
CO4	2	1	3	3	3	1	3	-	3
CO5	2	1	3	3	3	1	3	-	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	Performance in practical classes			Model Practical Examination	Attendance		
	Conduction of practical	Record work	viva				
Marks	15	5	5	15	10	50	100

Department	Electronics and Communication Engineering				Programme: **M.Tech.- VLSI & ES**			
Semester	**II**				Course Category: **PC**		End Semester Exam Type: **LE**	
Course Code	**P23HSPC02**				Periods/Week		Credit	Maximum Marks
					L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Seminar on ICT: A Hands-on approach**				0	0	4	2	50	50	100
Common to all M.Tech Programmes (ECE and VLSI & ES)											
Course Outcome	**On completion of the course, the students will be able to**										**BT Level**
	CO1	Select a topic, narrowing the topic into presentation.									4
	CO2	State an objective and use the relevant ICT tools to make the presentation effective.									4
	CO3	Study the topic and understanding the contributions and prepare report.									4
	CO4	Prepare a working demo.									3
	CO5	Prepare conclusions based on the reading of the topic and giving final Presentation.									3

The methodology used is “learning by doing”, a hands-on approach, enabling the students to follow their own pace. The teacher, after explaining the project, became a tutor, answering questions and helping students on their learning experience.

ICT skills

- Understand ICT workflow in the respective domain choose.
- Manage multitasking.
- Deal with main issues using tech in class.
- Record, edit and deliver audio and video.
- Automate assessments and results.

Scope

- Perspective in order to design activities in class.
- Understand the process of creating audiovisuals.

Teaching tools

- Different ways to create audiovisual activities.
- Handle audiovisual editors.
- Collaborative working.
- Individualize learning experience.
- Get instant feedback from students.

Each one of the students will be assigned an ICT Topic and the student has to conduct a detailed study on the assigned topic and prepare a report, running to 30 or 40 pages for which a demo to be performed followed by a brief question and answer session. The demo will be evaluated by the internal assessment committee (comprising of the Head of the Department and two faculty members) for a total of 100 marks.

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PSO1**	**PSO2**	**PSO3**
1	-	3	1	1	3	3	3	-	-
2	-	3	1	1	3	2	3	-	-
3	-	3	1	1	3	2	3	-	-
4	-	3	1	1	3	2	3	-	-
5	-	3	1	1	3	2	3	-	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)				Attendance	End Semester Examination (ESE) Marks	Total Marks
	Weekly Progress	Seminar	Record work	Viva			
Marks	40	30	10	10	10	-	100

PROFESSIONAL ELECTIVE COURSES		
Professional Elective–II (Offered in Semester II)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC01	Design of Analog and Mixed VLSI Circuits
2	P23VEEC02	Internet of Things and its Implementation
3	P23VEE206	Modeling and Synthesis with Verilog HDL
4	P23VEE207	Advanced Embedded System
5	P23VEE208	Distributed Embedded Computing

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. - VLSI & ES**						
Semester	**II**	Course Category: **PE**			End Semester Exam Type **TE**			
Course Code	**P23VEEC01**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Design of Analog and Mixed VLSI Circuits**	3	0	0	3	40	60	100

Common to all the M.Tech (ECE and VLSI & ES)

Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Distinguish the concept of analog integrated circuits of ADC and DAC Specifications.	**K3**
	CO2	Demonstrate the concept of Architecture of data converter.	**K3**
	CO3	Contrast the about SNR in data Converter and filters.	**K3**
	CO4	Discover the concept of operational amplifiers and mixed signal circuits.	**K3**
	CO5	Operation and features of Phase locked loop mixed mode VLSI circuits and differential amplifier.	**K4**

Unit - I	**Data Converters**	**Periods: 9**
Data Converter Fundamentals: Analog versus digital discrete time signals - converting analog signals to data signals- sample and hold characteristics - DAC specifications - ADC specifications - mixed-signal layout issues.		**CO1**
Unit - II	**Data Converter Architectures**	**Periods: 9**
Data Converter Architectures: DAC architectures - digital input code - resistors string - R-2R ladder networks -current steering - charge scaling – DACs - cyclic DAC - pipeline DAC - ADC architectures – flash ADC - 2-step flash ADC - pipeline ADC - integrating ADC - successive approximation ADC		**CO2**
Unit - III	**SNR in Data Converters**	**Periods: 9**
Data Converter SNR: Improving SNR using averaging (Excluding Jitter & averaging onwards) - decimating filters for ADCs (Excluding Decimating without averaging onwards) - interpolating filters for DAC - band pass and high pass sync. Filters.		**CO3**
Unit - IV	**Operational Amplifiers and Mixed Signal Circuits**	**Periods: 9**
Differential amplifier- basic differential pair - Gilbert Cell; Op-Amp: Performance parameters - one stage and two stage Op-Amp - design of two stage Op-Amps - gain boosting - common mode Feedback – slew rate – offset effects –PSRR- noise – stability and frequency compensation - two stage open loop comparators– high speed comparators - sample and hold circuit- switched capacitor circuits - oscillators - VCO - PLL.		**CO4**
Unit - V	**Instructional Activities**	**Periods: 9**
Design and simulation of different VLSI Circuits: Current mirrors - Differential Amplifier - PLL - ADC/DAC		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Razavi B, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill Edition, 2008.
2. Baker R J, “CMOS: Circuit Design, Layout and Simulation”, 3rd Edition, John Wiley and Sons, NJ, 2010
3. Karl Stephan, “Analog and Mixed-Signal Electronics”, John Wiley and Sons, 2015
4. Mourad Fakhfakh, Esteban Tlelo-cuautle and Rafael Castro-Lopez, “Analog/RF and Mixed-Signal CircuitSystematic Design”, Springer-Verlag Berlin and Heidelberg GmbH & Co. KG, 2015

Web References

1. http://nptel.ac.in/courses/117101105/
2. http://nptel.ac.in/courses/117101106/
3. http://nptel.ac.in/courses/117106034/
4. https://freevideolectures.com/course/3676/cmos-mixed-signal-vlsi-design

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	3	-
2	2	-	3	3	-	1	3	3	-
3	2	-	3	3	-	1	3	3	-
4	2	-	3	3	-	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. VLSI & ES**						
Semester	**II**	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEEC02**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Internet of Things and its Implementation**	**3**	**0**	**0**	**3**	40	60	100

Common to all the M.Tech (ECE and VLSI & ES)

Course Outcome		**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1	Articulate the main concepts, key technologies, strength and limitations of IoT	**K2**
	CO2	Identify the architecture, infrastructure models of IoT	**K2**
	CO3	Analyze the networking and how the sensors are communicated in IoT.	**K3**
	CO4	Analyze and design different models for IoT implementation.	**K3**
	CO5	Identify and design the new models for market strategic interaction.	**K3**

Unit-I	**Introduction to Internet of Things & UML**	**Periods: 9**
Rise of the machines – Evolution of IoT – Web 3.0 view of IoT – Definition and characteristics of IoT – IoT Enabling Technologies – IoT Architecture -– Fog, Edge and Cloud in IoT – Functional blocks of an IoT ecosystem –Smart Objects and Connecting Smart Objects - IoT levels and deployment templates. Overview of Unified Modeling Language (UML). IoT Models: Domain Model, Information Model, Functional Model, Communication Model, Security Model.		**CO1**
Unit-II	**Middleware and Protocols of IOT**	**Periods: 9**
Middleware architecture of RFID, WSN, SCADA, M2M –Interoperability challenges of IoT-Protocols for RFID, WSN, SCADA, M2M- Zigbee, KNX, BAC Net, MODBUS - Challenges Introduced by 5G in IoT Middleware (Technological Requirements of 5G Systems - Perspectives and a Middleware Approach Toward 5G (COMPaaS Middleware) – Resource management in IoT		**CO2**
Unit-III	**Communication and Networking**	**Periods: 9**
IoT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and LoRaWAN – Network Layer: IP versions, Constrained Nodes and Constrained Networks – Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks		**CO3**
Unit-IV	**IOT Implementation Tools**	**Periods: 9**
Introduction to Python, Introduction to different IoT tools, developing applications through IoT tools, developing sensor-based application through embedded system platform, Implementing IoT concepts with python, Implementation of IoT with Raspberry Pi		**CO4**
Unit-V	**Instructional Activities**	**Periods: 9**
Home automations - Smart cities – Environment – Energy – Retail – Logistics – Agriculture – Industry - Health and lifestyle – Case study.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Honbo Zhou, “Internet of Things in the cloud:A middleware perspective”, CRC press, 2012.
2. Vijay Madisetti and Arshdeep Bahga, “Internet of Things (A Hands-onApproach)”, VPT, 1st Edition, 2014.
3. Holler, Jan., Tsiatsis, Vlasios., Mulligan, Catherine., Karnouskos, Stamatis., Avesand, Stefan., Boyle, David. Internet of Things. Netherlands: Elsevier Science, 2014.
4. Pethuru Raj and Anupama C. Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press, 2017.

Web References

1. http://www.abouttheinternetofthings.com/category/iot-features/
2. https://nptel.ac.in/courses/106/105/106105166/

3. https://lecturenotes.in/subject/370/internet-of-things-iot
4. https://www.codeproject.com/Learn/IoT/

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	-	3
2	2	-	3	3	-	1	3	-	3
3	2	-	3	3	-	1	3	-	3
4	2	-	3	3	-	1	3	-	3
5	2	2	3	3	2	1	3	-	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. - VLSI & ES**						
Semester	**II**	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE206**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Modeling and Synthesis with Verilog HDL**	3	0	0	3	40	60	100

Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Recognize the basic conventions of Verilog HDL.	**K3**
	CO2	Define the various delay models of behavioral level description.	**K3**
	CO3	Synthesize the combinational and sequential circuits using Verilog HDL.	**K4**
	CO4	Synthesize the digital circuits using Switch level modeling.	**K4**
	CO5	Carryout the HDL for various higher end circuits using CAD tool.	**K4**

Unit - I	**Hardware Modeling with Verilog HDL**	**Periods: 9**
HDLs in EDA, System C, VHDL and Verilog, System Verilog overview, Hardware Encapsulation, Hardware Modeling with Verilog HDL, Hierarchical descriptions of hardware, Structured design methodology, Arrays, Using Verilog for synthesis, Event driven simulation and test benches, Logic system, data types and operators, User-defined primitives: Combinational behaviour, Sequential behavior.		**CO1**
Unit - II	**Delay Models & Behavioral Description**	**Periods: 9**
Verilog models of propagation delay, Built-in constructs, Inertial delay, Time scales and precision, Delays, Delay effects and Pulse rejection, Race condition in Verilog, Types of race condition, Task and function, Events, Process control, Disable a block, Watchdog, debugging, Code coverage, Testing strategies, File handling, Behavioral descriptions in Verilog HDL.		**CO2**
Unit - III	**Synthesis of Combinational Logic &Sequential Logic**	**Periods: 9**
Synthesis of Combinational Logic, HDL-Based Synthesis, Technology-Independent Design, Synthesis Methodology, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three-State Buffers, Outputs and Don't Cares, Synthesis of Sequential Logic, Latches, Edge-Triggered Flip- Flops, Registered Combinational Logic, Shift Registers and Counters		**CO3**
Unit - IV	**Synthesis of Language Constructs & Switch Level Model**	**Periods: 9**
Synthesis of Language constructs, MOS Transistor Technology, Switch-Level Models, PULL gates, CMOS Transmission gates, Bi-Directional gates (Switches), Signal Strengths, Strength Reduction by Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic		**CO4**
Unit - V	**Instructional Activities**	**Periods: 9**
Case Studies on VLSI Design Automation tools-An overview of the features of practical CAD tools – Modelsim - Leonardo spectrum -Xilinx ISE - Quartus II - VLSI backend tools –IC Station, Cadence and Synopsis.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. M,D,Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, Prentice Hall, 2006
2. Steven M. Rubin, “Computer Aids for VLSI Design”, http://www.rulabinsky.com/cavd (free online book),1997.
3. M,G, Arnold, “Verilog Digital – Computer Design”, Prentice Hall, 2006
4. Simon Monk, ‘Programming FPGAs: Getting Started with Verilog’, McGraw-Hill Education, 2016

Web References

1. http://web.ewu.edu
2. http://nptel.iitm.ac.in
3. http://www.asic-world.com/verilog/veritut.html
4. https://www.intel.com/content/www/us/en/programmable/support/training/course/ohdl1120.html

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	3	-
2	2	-	3	3	-	1	3	3	-
3	2	-	3	3	-	1	3	3	-
4	2	-	3	3	-	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. - VLSI & ES**						
Semester	**II**	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE207**	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	**Advanced Embedded System**	**3**	**0**	**0**	**3**	**40**	**60**	**100**

Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Insight into the significance of the role of embedded system for automotive applications.	**K3**
	CO2	Illustrate the need, choice of sensors and actuators and interfacing with ECU	**K3**
	CO3	Develop the Embedded concepts for vehicle management and control systems	**K3**
	CO4	Demonstrate the need of Electrical vehicle and able to apply the embedded system technology for various aspects of EVs	**K3**
	CO5	Improved Employability and entrepreneurship ability due to knowledge up gradation on recent trends in embedded systems design and its application in automotive systems.	**K3**

Unit - I	**Basic of Electronic Engine Control Systems**	**Periods: 9**
Overview of Automotive systems, fuel economy, air-fuel ratio, emission limits and vehicle performance; Automotive microcontrollers- Electronic control Unit- Hardware & software selection and requirements for Automotive applications – open source ECU- RTOS - Concept for Engine management-Standards; Introduction to AUTOSAR and Introduction to Society SAE- Functional safety ISO 26262- Simulation and modeling of automotive system components.		**CO1**
Unit - II	**Sensors and Actuators for Automotive**	**Periods: 9**
Review of sensors- sensors interface to the ECU, conventional sensors and actuators, Modern sensor and actuators - LIDAR sensor- smart sensors- MEMS/NEMS sensors and actuators for automotive applications		**CO2**
Unit - III	**Vehicle Management Systems**	**Periods: 9**
Electronic Engine Control-engine mapping, air/fuel ratio spark timing control strategy, fuel control, electronic ignition- Adaptive cruise control - speed control-anti-locking braking system-electronic suspension - electronic steering , Automatic wiper control- body control system ; Vehicle system schematic for interfacing with EMS, ECU. Energy Management system for electric vehicles- Battery management system, power management system-electrically assisted power steering system Adaptive lighting system- Safety and Collision Avoidance.		**CO3**
Unit - IV	**Onboard Diagnostics and Telematics**	**Periods: 9**
On board diagnosis of vehicles -System diagnostic standards and regulation requirements Vehicle communication protocols Bluetooth, CAN, LIN, FLEXRAY, MOST, KWP2000 and recent trends in vehicle communications- Navigation- Connected Cars technology – Tracking- Security for data communication- dashboard display and Virtual Instrumentation, multimedia electronics- Role of IOT in Automotive systems		**CO4**
Unit - V	**Instructional Activities**	**Periods: 9**
Simulation and modeling of automotive system components - Designing a Smart Sensor Network- Implementation of Vehicle Communication Protocols		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. William B. Ribbens," Understanding Automotive Electronics", Elseiver,2012
2. Jack Erjavec,JeffArias,"Alternate Fuel Technology-Electric ,Hybrid& Fuel Cell Vehicles",Cengage ,2012.
3. Tom Denton,"Automotive Electricals / Electronics System and Components", 3 rd Edition, 2004.

4. Uwe Kiencke, Lars Nielsen, “Automotive Control Systems: For Engine, Driveline, and Vehicle”, Springer; 1 edition, March 30, 2000.

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1. https://archive.nptel.ac.in/courses/107/106/107106088/
2. https://edisciplinas.usp.br/pluginfile.php/7518064/mod_resource/content/1/Automotive%20Electronics.pdf
3. https://training.uplatz.com/online-it-course.php?id=automotive-electrics-and-automotive-electronics-469
4. https://www.udemy.com/course/basics-of-automotive-electronics/

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	-	2	1	1	-	2	2	2	-
2	2	3	2	2	2	3	2	2	-
3	3	3	3	3	3	2	2	2	-
4	3	3	3	3	3	2	2	2	-
5	3	3	3	3	3	2	2	2	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. - VLSI & ES**						
Semester	**II**	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE208**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Distributed Embedded Computing**	3	0	0	3	40	60	100

Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Distinguish the concept of internet infrastructure and network security.	**K3**
	CO2	Demonstrate the concept of server applications and design a HTML & XML Web page.	**K3**
	CO3	Contrast embedded systems by using java and j2ME in web technology.	**K3**
	CO4	Discover the embedded agents for various criteria with benchmark embedded.	**K3**
	CO5	Gain knowledge in distributed embedded computing architecture.	**K4**

Unit - I	**Internet Infrastructure**	**Periods: 9**
Broad Band Transmission facilities –Open Interconnection standards –Local Area Networks – Wide AreaNetworks –Network management – Network Secuity – Cluster computers.		**CO1**
Unit - II	**Internet Concepts**	**Periods: 9**
Capabilities and limitations of the internet -– Interfacing Internet server applications to corporate databasesHTML and XML Web page design through programming and the use of active components.		**CO2**
Unit - III	**Embedded Java**	**Periods: 9**
Introduction to Embedded Java and J2ME - embedded java concepts -IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases –– Smart Card basics – Java card technology overview – Java card objects – Java card applets – Web Technology for Embedded Systems.		**CO3**
Unit - IV	**Embedded Agent**	**Periods: 9**
Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.		**CO4**
Unit - V	**Instructional Activities**	**Periods: 9**
Simulation of LANs, WANs, VPNs- Encryption protocols- Simulation of multi-threading application		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Bernd Kleinjohann, “Architecture and Design of Distributed Embedded Systems”, Springer, 2014
2. Bernd Kleinjohann, K H (Kane) Kim and Lisa Kleinjohann, “Design and Analysis of Distributed EmbeddedSystems”, Springer, 2014
3. M.Teresa Higuera-Toledano and Andy J. Wellings, “Distributed, Embedded and Real-time Java Systems”,Springer-Verlag New York Inc., 2012
4. Wigglesworth,”Java Programming Advanced Topics,Cengage,2010

Web References

1. http://www.oracle.com/technetwork/articles/javase/rmi-corba-136641.html
2. http://www.es.ele.tue.nl/~heco/courses/ECA/index.html
3. www.pa.icar.cnr.it/cossentino/AOSETF10/docs/jamont.ppt
4. http://philip.greenspun.com/panda/databases-interfacing

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	-	3
2	2	-	3	3	-	1	3	-	3
3	2	-	3	3	-	1	3	-	3
4	2	-	3	3	-	1	3	-	3
5	2	2	3	3	2	1	3	-	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

PROFESSIONAL ELECTIVE COURSES		
Professional Elective–III (Offered in Semester II)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC03	System-on-Chip Design
2	P23VEE209	DSP Processor Architecture and Programming
3	P23VEE210	Design for Verification Using UVM
4	P23VEE211	Testing and Fault Diagnosis of VLSI Circuits
5	P23VEE212	Soft Computing

Department	Electronics and Communication Engineering			Programme: M.Tech. - VLSI & ES					
Semester	III			Course Category: PE			End Semester Exam Type: TE		
Course Code	P23VEEC03			Periods/Week			Credit	Maximum Marks	
				L	T	P	C	CAM	ESE	TM
Course Name	System-on-Chip Design			3	0	0	3	40	60	100
Common to all the M.Tech (ECE and VLSI & ES)										
Course Outcome	On completion of the course, the students will be able to							BT Mapping (Highest Level)		
	CO1	Memorize the system architecture, components of system hardware and software.						K2		
	CO2	Explain the basic concepts of processor architecture and instructions and delays.						K2		
	CO3	Describe external and internal memory of SOC and organization.						K2		
	CO4	Explain SOC customization and reconfiguration technologies.						K2		
	CO5	Apply the knowledge of SOC design in real time applications.						K3		

Unit - I	**Introduction**	**Periods: 9**
System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, an approach for SOC Design, System Architecture and Complexity.		CO1
Unit - II	**Processors**	**Periods: 9**
Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors,Superscalar Processors.		CO2
Unit - III	**Memory Design F for SOC**	**Periods: 9**
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split –I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction**.**		CO3
Unit - IV	**Interconnect Customization and Configuration**	**Periods: 9**
Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.		CO4
Unit - V	**Instructional Activities**	**Periods: 9**
SOC Design approach: simulate and verify AES algorithms, design and evaluation of Image compression JPEG compression.		CO5

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Books

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd. 2012.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., Addison Wesley Professional 2000.
3. D. C. Black, J. Donovan, B. Bunton, A. Keist, SystemC: From the Ground Up, Second Edition, Springer, 2010.
4. P. Marwedel, Embedded System Design: Embedded Systems Foundations of Cyber-Physical Systems, Third Edition, Springer, 2018.

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1. http://ic.sjtu.edu
2. http://nptel.iitm.ac.in
3. https://www.coursera.org/lecture/fpga-intro/programmable-system-on-chip-X5Gaq
4. https://ieeexplore.ieee.org/document/5490602

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	1	1	3	3	-
2	2	-	3	3	1	1	3	3	-
3	2	-	3	3	1	1	3	3	-
4	2	-	3	3	1	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. - VLSI & ES**						
Semester	**III**	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE209**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**DSP Processor Architecture and Programming**	3	0	0	3	40	60	100

Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Distinguish the various Data representations and Processors.	**K2**
	CO2 Construct and analysis of various architecture of TMS320C Series.	**K2**
	CO3 Compute and illustrate the Fast Fourier transform of TMS320C Series.	**K3**
	CO4 Explains and compares DFT & FFT of fixed- and floating-point representation.	**K3**
	CO5 Summaries the various algorithms for real world applications.	**K4**

Unit - I	**Digital Signal Processing Systems**	**Periods: 9**
Introduction to Digital signal processor architectures – Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.		CO1
Unit - II	**Digital Signal Processors**	**Periods: 9**
TMS320C62x AND TMS320C64x - Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Real time implementations.		CO2
Unit - III	**Implementation of Fast Fourier Transforms**	**Periods: 9**
Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.		CO3
Unit - IV	**Fir and LIR Filter Implementations**	**Periods: 9**
FIR and IIR filters – Characteristics, Structures, FIR Filter design using Windowing and frequency sampling method, IIR Filter-Butterworth and Chebyshev Filter Design-, Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.		CO4
Unit - V	**Instructional Activities**	**Periods: 9**
Design a FIR, IIR filter and implement in DSP processor. Develop programs to perform various process of convolution, DFT, FFT algorithm. Digital Signal Processor based experiments: Auto Correlation and Cross correlation. Linear and circular Convolution. DFT/FFT. Design of FIR filter. Design of IIR filter		CO5

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. John G Proakis and Manolakis, “Digital Signal Processing Principles, Algorithms and Applications”, Pearson, Fourth Edition, 2007
2. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, Cengage Learning India Private Limited, Delhi 2012.
3. Rulph Chassaing and Donald Reay, Digital Signal Processing and Applications with the C6713 and C6416 DSK, John Wiley and Sons, Inc., Publication, 2012.
4. A.V. Oppenheim, R.W.Schafer and J.R.Buck, "Discrete Time Signal Processing", Pearson, 2004.

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1. http://www.nptel.iitm.ac.in/courses
2. https://link.springer.com
3. http://users.ece.utexas.edu/~bevans/hp-dsp-seminar/01_Introduction
4. http://meseec.ce.rit.edu/eecc722-fall2003/722-10-8-2003

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	-	3
2	2	-	3	3	-	1	3	-	3
3	2	-	3	3	-	1	3	-	3
4	2	-	3	3	-	1	3	-	3
5	2	2	3	3	3	1	3	-	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech**. - **VLSI & ES**						
Semester	**III**	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE210**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Design for Verification Using UVM**	3	0	0	3	40	60	100

Course Outcome	On completion of the course, the students will be able to	BT Mapping (Highest Level)
	CO1 Understand the basic concepts of two methodologies UVM	**K2**
	CO2 Build actual verification components.	**K3**
	CO3 Generate the register layer classes.	**K3**
	CO4 Code testbenches using UVM.	**K3**
	CO5 Understand advanced peripheral bus testbenches.	**K3**

UNIT-I	**Introduction**	**Periods: 9**
Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation		CO1
UNIT-II	**Developing Reusable Verification Components**	**Periods: 9**
Modeling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage		CO2
UNIT-III	**UVM Using Verification Components**	**Periods: 9**
Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes -Verification Component Configuration - Creating and Selecting a User-Defined Test - Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards- Implementing a Coverage Model		CO3
UNIT-IV	**UVM Using the Register Layer Classes**	**Periods: 9**
Using the Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register-Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre-Defined Sequences		CO4
UNIT-V	**Instructional Activities**	**Periods: 9**
Implementation of Memory Transfer using Verilog-Test classes- Interfacing using DUT- Register class modelling		CO5

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 09**

Reference Books

1. The UVM Primer, An Introduction to the Universal Verification Methodology, Ray Salemi,2013.
2. Chris Spear, Greg Tumbush," System Verilog for Verification: A Guide to Learning the Testbench Language Features"3rd edition, 2012.
3. Rosenberg, Sharon, and Meade, Kathleen. A Practical Guide to Adopting the Universal Verification Methodology (UVM) Second Edition. United Kingdom, Lulu.com, 2012.
4. Rosenberg, Sharon, and Meade, Kathleen A. A Practical Guide to Adopting the Universal Verification Methodology (UVM). United States, Cadence Design Systems, 2010.

Web References

1. https://www.chipverify.com/uvm/uvm-tutorial
2. https://verificationguide.com/uvm/uvm-testbench-architecture/
3. https://www.udemy.com/course/learn-ovm-uvm/
4. https://www.cadence.com/en_US/home/training/all-courses/82143.html

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	1	-	1	1	2	-	1	-	-
2	1	-	1	1	2	-	1	-	-
3	1	-	1	1	2	-	1	-	-
4	1	-	1	1	2	1	1	-	-
5	1	-	1	1	2	1	1	-	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: M.Tech. VLSI & ES						
Semester	III	Course Category: PE			End Semester Exam Type: TE			
Course Code	P23VEE211	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	Testing and Fault Diagnosis of VLSI Circuits	3	0	0	3	40	60	100

Course Outcome	On completion of the course, the students will be able to	BT Mapping (Highest Level)
	CO1 Interpret the different types of fault models	**K2**
	CO2 Generate test patterns to detect the fault in combinational circuits	**K3**
	CO3 Generate test patterns to detect the fault in sequential circuits	**K3**
	CO4 Design a circuit for testability	**K3**
	CO5 Infer the different measures of system diagnosable	**K2**

UNIT-I	**Fault Modeling and Simulation**	**Periods: 9**
Defect, errors and faults- Functional versus structural testing-Levels of fault models- Single stuck at fault-Modeling circuits for simulation- Algorithms for true-value simulation- Algorithms for fault simulation- Statistical methods for fault simulation		CO1
UNIT-II	**Test Generation of Combinational Circuits**	**Periods: 9**
Algorithms and representation- Redundancy identification- Testing as a global problem-Combinational ATPG algorithm-D-algorithm-PODEM-FAN-Test generation Systems-Test compaction.		CO2
UNIT-III	**Test Generation of Sequential Circuits**	**Periods: 9**
ATPG for single clock synchronous circuits - Time-Frame expansion method - Simulation based sequential circuit		CO3
UNIT-IV	**Design for Testability**	**Periods: 9**
Testability –AdHoc design for testability techniques- Controllability and observability by means of scan registers- Generic scan-based design- Classical scan designs- Board level and system level DFT approaches-Boundary scan standards		CO4
UNIT-V	**Instructional Activities**	**Periods: 9**
Implementation of D-algorithm- Categorization of faults in schematic- Generation of test Patterns-Design of simple circuits with scan registers		CO5

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Books

1. Bushnell M.L. and Agrawal V.D., “Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI Circuits”, Kluwer Academic Publishers, 2nd Printing, 2005.
2. Liu, Ruey-wen. Testing and Diagnosis of Analog Circuits and Systems. United States, Springer US, 2012.
3. Abramovici, M., Breuer, M.A and Friedman, A.D., “Digital Systems and Testable Design”, Jaico Publishing House, 13th Impression, 2012.
4. Laung – Terng wang, Cheng – wen wu, Xidogingwen, “VLSI Testing Principles and Architectures: Design for Testability”, Morgan Kaufmann Publisher,2nd Reprint, 2013.

Web References

1. https://onlinecourses.nptel.ac.in/noc20_ee76/preview
2. https://nptel.ac.in/courses/117105137
3. https://archive.nptel.ac.in/courses/106/103/106103116/
4. https://archive.nptel.ac.in/content/storage2/courses/106103116/handout/mod1.pdf

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	3	1	1	-	-	-	1	-	-
2	3	2	1	-	-	-	1	-	-
3	3	2	1	-	-	-	1	-	-
4	3	2	1	-	2	-	1	-	-
5	2	1	1	-	-	-	1	-	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: **M.Tech. - VLSI & ES**						
Semester	**III**	Course Category: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE212**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Soft Computing**	3	0	0	3	40	60	100

Course Outcome		**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1	Explain the fundamental theory and concepts of neural networks, Identify different neural network architectures, algorithms, applications and their limitations.	**K3**
	CO2	Apply fuzzy logic and reasoning to handle uncertainty and solve engineering problems.	**K3**
	CO3	Apply genetic algorithms to combinatorial optimization problems.	**K3**
	CO4	Design hybrid system to revise the principles of soft computing in various applications.	**K3**
	CO5	Apply modern software tools to solve real problems using a soft computing approach and evaluatevarious soft computing approaches for a given problem.	**K3**

Unit - I	**Neural Network**	**Periods: 9**
Basic concept - mathematical model - properties of neural networks - architectures - different learning methods - common activation functions - application of neural networks; Neuron architecture: Algorithms - McCullo h-Pitts - Back propagation NN - ADALINE - MADALINE - Discrete Hopfield net - BAM - Maxnet.		CO1
Unit - II	**Fuzzy Sets & Logic**	**Periods: 9**
Fuzzy versus Crisp - fuzzy sets - fuzzy relations - laws of propositional logic - inference - Predicate logic fuzzylogic - quantifiers - inference - defuzzification methods.		CO2
Unit - III	**Genetic Algorithm**	**Periods: 9**
Role of GA - fitness function - selection of initial population - cross over (different types) - mutation – inversion - deletion - constraints handling and applications of travelling salesman and graph coloring.		CO3
Unit - IV	**Hybrid Systems**	**Periods: 9**
Hybrid Systems: GA based BPNN (Weight determination) - Neuro fuzzy systems - Fuzzy BPNN - fuzzyneuron - architecture - learning - Fuzzy logic controlled genetic algorithm		CO4
Unit - V	**Instructional Activities**	**Periods: 9**
Simulation of PSD - HSA and ACO related to either wireless networking or Antenna or Image Processingusing related tools.		CO5

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. S.N. Sivanandam, S.N. Deepa, “Principles of Soft Computing”, 2nd Edition, John Wiley India, 2012.
2. S. Haykin, “Neural Networks - A Comprehensive Foundation”, 2nd Edition, Pearson Education, 2005.
3. T.S. Rajasekaran, G.A. VijaylakshmiPai, “Neural Networks, Fuzzy Logic & Genetic Algorithms – Synthesis and Applications”, Prentice-Hall India, 2003.
4. David E. Goldberg, Genetic Algorithm in Search Optimization and Machine Learning Pearson EducationIndia, 2013

Web References

1. http://www.vssut.ac.in/lecture_notes/lecture1423723637.pdf
2. https://lecturenotes.in/subject/124/soft-computing-sc
3. https://nptel.ac.in/courses/106/105/106105173/
4. https://www.tutorialspoint.com/fuzzy_logic/index.htm

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	1	1	3	-	2
2	2	-	3	3	1	1	3	-	2
3	2	-	3	3	1	1	3	-	2
4	2	-	3	3	1	1	3	-	2
5	2	2	3	3	2	1	3	-	2

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

SEMESTER – III

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23VEE3XX	Professional Elective - IV	PE	3	0	0	3	40	60	100
2	P23VEE3XX	Professional Elective - V	PE	3	0	0	3	40	60	100
3	P23VEE3XX	Professional Elective - VI	PE	3	0	0	3	40	60	100
Project Work										
4	P23VEW301	Project Phase - I	PA	0	0	12	6	50	50	100
5	P23VEW302	Internship	PA	0	0	0	2	100	0	100
Ability Enhancement Course										
6	P23VEC301	NPTEL / SWAYAM / MOOC	AEC	0	0	0	-	100	0	100
Total							**17**	**370**	**230**	**600**

PROFESSIONAL ELECTIVE COURSES		
Professional Elective–IV (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC04	Real Time Operating System
2	P23VEEC05	Cloud computing and Distributed System
3	P23VEE313	VLSI Signal Processing
4	P23VEE314	High Speed Digital Design
5	P23VEE315	Nanoelectronics

Department	**Electronics and Communication Engineering**	Programme: **M.Tech VLSI & ES**						
Semester	**III**	Course Category Code: **PE**			End Semester Exam Type: **TE**			
Course Code	**P20VEEC04**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Real Time Operating System**	3	0	0	3	40	60	100

Common to all the M.Tech (ECE and VLSI & ES)

Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Define and demonstrate understanding of key real-time system terminology and design issues.	**K2**
	CO2 Analyze and compare process scheduling algorithms (round robin, fixed priority, dynamic priority) considering real-time constraints, and choose the optimal one for specific needs.	**K4**
	CO3 Implement mechanisms for enforcing mutual exclusion and protecting critical sections to guarantee correct system behavior.	**K3**
	CO4 Understand the architecture and operation of Windows CE and polled loop systems, identifying their suitability for specific real-time applications.	**K2**
	CO5 Design and implement real-time control systems using embedded hardware (e.g., CAN bus) and RTOS capabilities to achieve desired behaviors and meet real-time constraints.	**K3**

Unit-I	**Basic real time concepts**	**Periods: 9**
Terminologies – Real time system design issues – Hardware Developments – Hardware Interfacing – CPU – RISC vs CISC – Memory Access – Memory Organization – Direct Memory Access – Memory Mapped Input/output – Pipelining – Coprocessors.		**CO1**
Unit-II	**Real time operating systems**	**Periods: 9**
Real Time Kernels: Pseudokernels, Interrupt Driven Systems, Hybrid Systems – Theoretical Foundations of Real Time Operating Systems: Process scheduling – Round Robin Scheduling – Fixed Priority Scheduling – Dynamic Priority Scheduling – Buffering data – Time Relative buffering – Queues – Semaphores.		**CO2**
Unit-III	**Resources - resource access control**	**Periods: 9**
Enforcement of mutual exclusion and critical sections – Resource Conflicts and Blocking – Effects of Resource contention and Resource Access Control: Priority Inversion, Timing Anomalies, Deadlock – Non Preemptive Critical Sections – Basic Priority Inheritance Protocol – Basic Priority Ceiling Protocol.		**CO3**
Unit-IV	**WinCE**	**Periods: 9**
Introduction WinCE, Polled Loop Systems - RTOS Porting to a Target, Explanation of Application, Kernel, OAL, Explanation of CPU, SOC, Platform, MMU, MMU for ARM based devices in WinCE, Comparison of µCos-II, Embedded Linux, Real Time Linux, Vx-Works, QNX Nutrino, ThreadEX		**CO4**
Unit-V	**Instructional Activities**	**Periods: 9**
Design and simulate static & dynamic scheduling algorithms in suitable platform. Simulation of RTOS for the application of Engine Management System using CAN protocols or GNU gcc *tools.*		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Book

1. Phillip A. Laplante, “Real Time System Design and Analysis”, John Wiley & Sons Publications, 2004.
2. Jane W.S. Liu, “Real Time Systems”, Prentice Hall, 2000.
3. Samuel Phuns, Professional Windows Embedded CE 6.0, Wrox, 2008.
4. Rajkamal, Embedded System, Tata McGraw Hill, 2003.

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1. http://www.nptel.iitm.ac.in
2. http://www.ocw.mit.edu.
3. http://web.iiit.ac.in/~bezawada/CN.html
4. https://www.tutorialspoint.com/Real-Time-Embedded-Systems

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

Cos	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	1	1	3	-	2
2	2	-	3	3	1	1	3	-	2
3	2	-	3	3	1	1	3	-	2
4	2	-	3	3	1	1	3	-	2
5	2	2	3	3	2	1	3	-	2

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech VLSI & ES**						
Semester	**III**	Course Category Code: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEEC05**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Cloud Computing and Distributed Systems**	**45**	**0**	**0**	**3**	**40**	**60**	**100**

Common to all the M.Tech (ECE and VLSI & ES)

Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Understand cloud computing architecture and deployment model.	**K3**
	CO2 Outline cloud service models and Interconnection networks.	**K2**
	CO3 Implement Parallel and Distributed Programming Models.	**K3**
	CO4 Deploy applications over commercial cloud computing infrastructures	**K3**
	CO5 Solve a real-world problem using cloud computing through group collaboration.	**K4**

Unit-I	**Cloud Architecture**	**Periods: 9**
Cloud Computing Infrastructure- Cloud Computing Types- Service Architecture- Cloud Computing Reference Model- Cloud System Architecture- Cloud Deployment Model- Basic Principles- Two-layer Connectivity for Cloud Federation- Cloud Ecosystem Model- Cloud Unified Process.		**CO1**
Unit-II	**Cloud Service Models**	**Periods: 9**
Service Models: Public, Private, and Hybrid Clouds- Platform-as-a-Service (PaaS)-Data-Center Design and Interconnection Networks: Warehouse-Scale Data-Center Design-Data Center Interconnection Networks- A Generic Cloud Architecture Design -Architectural Design Challenges.		**CO2**
Unit-III	**Distributed System Models**	**Periods: 9**
Clusters of Cooperative Computers-Cloud Computing over the Internet-Software Environments: Service-Oriented Architecture (SOA)-Parallel and Distributed Programming, Performance Metrics and Scalability Analysis -Energy Efficiency in Distributed Computing.		**CO3**
Unit-IV	**Programming Paradigms**	**Periods: 9**
Parallel and Distributed Programming Paradigms-MapReduce, Twister and Iterative MapReduce-Hadoop Library from Apache-Dryad and DryadLINQ from Microsoft-Sawzall and Pig Latin High-Level Languages-Mapping Applications to Parallel and Distributed Systems.		**CO4**
Unit-V	**Instructional Activities**	**Periods: 9**
Programming Support of Google App Engine-Amazon AWS and Microsoft Azure - Open-Source Eucalyptus, Nimbus, Open Nebula, Sector/Sphere and Open Stack.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Kai Hwang, Jack Dongarra, Geoffrey C. Fox “Distributed and Cloud Computing: From Parallel Processing to the Internet of Things”,2011
2. A. Srinivasan, J. Suresh, “Cloud Computing: A Practical Approach for Learning And Implementation”, Pearson,2014
3. Thomas Erl, Ricardo Puttini, Zaigham Mahmood "Cloud Computing Concepts, Technology & Architecture", Pearson Education (US),2013.
4. Frank M. Groom, Stephan S. Jones, "Enterprise Cloud Computing for Non-Engineers", Taylor & Francis Ltd, CRC Press, 2018

Web References

1. https://www.iare.ac.in/sites/default/files/lecture_notes/CC%20LECTURE%20NOTES.pdf

2. https://nptel.ac.in/courses/106/105/106105167/
3. https://mrcet.com/downloads/digital_notes/CSE/IV%20Year/CLOUD%20COMPUTING%20NOTES.pdf
4. https://nptel.ac.in/courses/106/106/106106107/

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	2	1	2	-	2
2	2	-	3	3	2	1	2	-	2
3	2	-	3	3	2	1	2	-	2
4	2	-	3	3	2	1	2	-	2
5	2	2	3	3	2	1	2	-	2

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: M.Tech VLSI & ES						
Semester	III	Course Category Code: PE			End Semester Exam Type: ES			
Course Code	P23VEE313	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	VLSI Signal Processing	3	0	0	3	40	60	100

Course Outcome	On completion of the course, the students will be able to	BT Mapping (Highest Level)
	CO1 Understand VLSI design methodology for signal processing systems.	K2
	CO2 Design an application off Unfolding in Signal processing	K3
	CO3 Design Systolic Design for Space Representations	K3
	CO4 Implement VLSI algorithms in DSP.	K4
	CO5 Implement basic architectures for DSP using CAD tools	K4

Unit-I	Pipelining And Parallel Processing	Periods: 9
Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques..		CO1
Unit-II	**Unfolding And Retiming Application Of Unfolding**	**Periods: 9**
Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.		CO2
Unit-III	**Fast Convolution**	**Periods: 9**
Fast Convolution: Introduction, Cook, Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection		CO3
Unit-IV	**Systolic Architecture Design**	**Periods: 9**
Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.		CO4
Unit-V	**Instructional Activities**	**Periods: 9**
Implement basic architectures for DSP using CAD tools, Study of Synopsys VCS simulation tool for verification of digital signal processing algorithms and architectures.		CO5

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Books

1. Keshab K. Parhi. VLSI Digital Signal Processing Systems, Wiley-Inter Sciences, 2008
2. Durgesh Nandan,Basant Kumar Mohanty), Sanjeev Kumar , VLSI Architecture for Signal, Speech, and Image Processing,Apple Academic Press,Taylor and Francis 2023.
3. Mahesh Mehendale, Sunil D. Sherlekar, “VLSI Synthesis of DSP Kernels Algorithmic and Architectural Transformations”,. Springer US, 2013.
4. Cosmin Radu Popa, “Synthesis of computational structures for analog signal processing”, Springer 2011

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1. https://archive.nptel.ac.in/courses/108/105/108105157
2. https://onlinecourses.nptel.ac.in/noc20_ee44/preview
3. https://ee.iitpkd.ac.in/node/61
4. https://lib.ui.ac.id/detail?id=20410828&lokasi=lokal

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	3	2	1	2	-	1	3	2	-
2	3	2	1	2	-	1	3	2	-
3	3	2	1	2	-	1	3	2	-
4	3	2	1	2	-	1	3	2	-
5	3	2	1	2	-	1	3	2	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech VLSI & ES**						
Semester	**III**	Course Category Code: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE314**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**High Speed Digital Design**	**3**	**0**	**0**	**3**	**40**	**60**	**100**

Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Explain the basic transmission concepts.	**K2**
	CO2 Relate power distribution and noise.	**K3**
	CO3 Describe the working of signaling circuits.	**K3**
	CO4 Illustrate the characteristic of timing convention and synchronization.	**K3**
	CO5 Able to determine optimization parameters through simulation.	**K4**

Unit-I	**Modelling And Analysis Of Wires**	**Periods: 9**
Modeling of wires, geometry and electrical properties of wires, Electrical models of wires, transmission lines, lossless LC transmission lines, lossy RLC transmission lines and special transmission lines.		**CO1**
Unit-II	**Power Distribution And Noise**	**Periods: 9**
Power supply network, local power regulation, IR drops, area bonding. On-chip bypass capacitors and symbiotic bypass capacitors. Power supply isolation. Noise sources in digital systems, power supply noise, crosstalk and inter symbol interference.		**CO2**
Unit-III	**Signaling Convention and Circuits**	**Periods: 9**
Signaling modes for transmission lines, signaling over lumped transmission media, signaling over RC interconnect, driving lossy LC lines, simultaneous bi-directional signaling terminations and transmitter and receiver circuits.		**CO3**
Unit-IV	**Timing Convention And Synchronization**	**Periods: 9**
Timing fundamentals, timing properties of clocked storage elements, encoding timing: signals and events, open loop timing, level sensitive clocking, pipeline timing, closed loop timing, clock distribution, synchronization failure and meta-stability, clock domains, clock synchronization.		**CO4**
Unit-V	**Instructional Activities**	**Periods: 9**
Simulation using CAD tools for characterizing wires, crosstalk in coupled lines, and measuring IC package parasitics.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. William S. Dally& John W. Paulton, Digital System Engineering, Cambridge University Press, 2008.
2. Stephen H. Hall, Garrett W. Hall & James A. McCall, High-Speed Digital System Design - A Handbook of Interconnect Theory and Design Practices, John Wiley & Sons, 2000
3. Stephen H. Hall & Howard L. Heck, Advanced Signal Integrity for High-Speed Digital Designs, John Wiley & Sons, 2009.
4. Masakazu Shoji, High Speed Digital Circuits, Addison Wesley Publishing Company, 2004.

Web References

1. https://pdfcoffee.com/digital-system-engineering-pdf-free.html
2. https://dl.icdst.org/pdfs/files3/ba72c65e020de8871cf4c9d09753d759.pdf
3. https://electronix.org.ru/books/high-speed-digital-design.pdf
4. https://www.keysight.com/us/en/assets/7123-1074/ebooks/End-to-End-High-Speed-Digital-Design.pdf

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	1	1	3	3	-
2	2	-	3	3	1	1	3	3	-
3	2	-	3	3	1	1	3	3	-
4	2	-	3	3	1	1	3	3	-
5	2	-	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: **M.Tech. VLSI & ES**						
Semester	**III**	Course Category Code: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE315**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Nanoelectronics**	**3**	**-**	**-**	**3**	**40**	**60**	**100**

Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Gain the advanced concepts of quantum theory and Understand the importance of Schrodinger wave equation & its applications	**K2**
	CO2 Building molecular-level devices and systems.	**K3**
	CO3 Design of Carbon-based Nano electronics devices and learn the fundamentals of Spintronics.	**K3**
	CO4 Summarize the types and applications of Nano electronics memories.	**K3**
	CO5 Able to use the optimization techniques to solve the real world problems	**K4**

Unit-I	**Quantum Mechanics, Free And Confined Electrons**	**Periods:9**
Origin of Quantum mechanics, Light as a wave and Particle-Electrons as a wave and Particle-wave packets and uncertainity-general postulates of Quantum mechanics- Schrodinger equation- free electrons, electrons confined to a boundary region of space and quantum Numbers, Fermi level and chemical potential, Partial confined electrons, Electrons confined to atoms ,Quantum Dots , Quantum Wires, Quantum Wells.		**CO1**
Unit-II	**Phenomenon Of Electron**	**Periods:9**
Kronig-Penny Model of band structure-Graphene and carbon nanotubes-Tunnel Junctions and application of Tunneling-coulomb blockade, single Electron Transistor- SET and FET Structures-Density of states –classical and Quantum statistics		**CO2**
Unit-III	**Nanowires, Ballistic Transport And Spin Transport**	**Periods:9**
Classical and semi classical transport-Ballistic Transport-Electron collision and length scales, ballistic transport model, quantum resistance and conductance, origin of the quantum resistance, carbon Nanotubes and Nanowires-Transport of spin and spintronics		**CO3**
Unit-IV	**Processing And Techniques Of Nanomaterials**	**Periods:9**
Methods for creating nanostructures –Vapor phase synthesis-liquid phase synthesis-sol-Gel technique-solid state phase synthesis-consolidation of Nanopowders		**CO4**
Unit-V	**Instructional Activities**	**Periods:9**
Simulation-Transfer characteristics of Single level molecule, single Electron Transistor and Field Effect Transistor.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. George W. Hanson, Fundamental of Nanoelectronics, Pearson education.2008.
2. Loutfy.H.Madkour,"Nanoelectronics Materials-Fundamentals of applications"springer,2019
3. Michael A. Nielsen and Isaac L. Chuang, "Quantum Computation and Quantum Information", Cambridge University Press, 2000.
4. Kiyoo Itoh Masashi Horiguchi, Hitoshi Tanaka, Ultra Low voltage nano scale memories. Spl Indian Edition,Springer.

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2. https://www.fisgeo.unipg.it/luca.gammaitoni/fisinfo/documenti-fisici/Electronics-beyond-nanoscale-cmos.pdf
3. https://scienceinfo.com/nanolithography-definition-techniques/
4. https://www.nanowerk.com/nanoelectronics.php

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	3	3	2	-	2	-	2	-	-
2	2	2	1	-	1	-	2	-	-
3	2	-	1	-	1	-	2	-	-
4	2	1	1	-	2	-	2	-	-
5	2	-	1	-	1	-	2	-	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

PROFESSIONAL ELECTIVE COURSES		
Professional Elective –V (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC06	Edge Computing
2	P23VEE316	CAD for VLSI Circuits
3	P23VEE317	Advanced Image Processing
4	P23VEE318	Hardware Software Co-Design
5	P23VEE319	Micro-Electromechanical Systems

Department	Electronics and Communication Engineering			Programme: M.Tech VLSI&ES			
Semester	III			Course Category Code: PE		End Semester Exam Type: TE	
Course Code	P23VEEC06	Periods/Week			Credit	Maximum Marks	
		L	T	P	C	CAM	ESE	TM
Course Name	Edge Computing	3	0	0	3	40	60	100

Common to all the M.Tech (ECE and VLSI & ES)

Course Outcome	On completion of the course, the students will be able to	BT Mapping (Highest Level)
CO1	Comprehend concepts on Edge computing and its deployment	K2
CO2	Comprehend concepts Edge Computing based on sensing and Internet connectivity	K2
CO3	Identify and describe the key architectural features of Edge Computing and their network	K2
CO4	Conceptualize applications implementing edge computing	K3
CO5	Identify and model Edge model using simulation tool	K2

Unit-I	IoT And Edge Computing Definition And Use Cases	Periods:9
Introduction to Edge Computing Scenario's and Use cases - Edge computing purpose and definition, Edge computing use cases, Edge computing hardware architectures, Edge platforms, Edge vs Fog Computing, Communication Models - Edge, Fog and M2M.		CO1
Unit-II	**IoT Architecture And Core IoT Modules**	**Periods:9**
A connected ecosystem,IoT versus machine-to-machine versus, SCADA, The value of a network and Metcalfe's and Beckstrom's laws, IoT and edge architecture, Role of an architect, Understanding Implementations with examples-Example use case and deployment, Case study – Telemedicine palliative care, Requirements, Implementation, Use case retrospective.		CO2
Unit-III	**Non-IP Based And IP-Based Wpan**	**Periods:9**
Non-IP Based WPAN ;802.15 standards, Zigbee, Z-wave, Bluetooth. IP-Based WPAN and WLAN, TCP/IP, WPAN with IP – 6LoWPAN, IEEE 802.11 protocols and WLAN, Edge to Cloud Protocols, MQTT, Constrained Application Protocol.		CO3
Unit-IV	**Security In Edge Devices**	**Periods:9**
IoT and Edge Security, Physical and hardware security, Shell security, Cryptography, Software-Defined Perimeter, Block chains and cryptocurrencies in IoT, Government regulations and intervention		CO4
Unit-V	**Instructional Activities**	**Periods:9**
Deploy IoT Edge module to a virtual Linux device. Deploy IoT Edge module to a Windows device. Principle of Installation of Linux Operating System porting. Use IoT edge device as a gateway. Edge computing with RaspberryPi,		CO5

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Books

1. Perry Lea," IoT and Edge Computing for Architects"-second edition, Packt, March,2020
2. Mohiuddin Ahmed (Editor), Paul Haskell-Dowland (Editor), "Secure Edge Computing: Applications, Techniques and Challenges", CRC press, first edition, August 2021.
3. Asoke K Talukder and Roopa R Yavagal, "Mobile Computing," Tata McGraw Hill, 2010
4. Fog and Edge Computing: Principles and Paradigms by Rajkumar Buyya, Satish Narayana Srirama,Wiley, January 2019

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1. https://www.youtube.com/watch?v=8WBPcfjftyw
2. http://acl.digimat.in/nptel/courses/video/106104242/L02.html
3. https://www.youtube.com/watch?v=ulCZQDUN0tc
4. https://www.youtube.com/watch?v=nPOUoJavYQc

* TE – Theory Exam, LE – Lab Exam

Dr. P. Raja, Chairman - Bos

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	3	2	1	-	2	-	1	3	1
2	3	2	1	-	2	-	1	3	1
3	3	2	1	-	2	-	1	3	1
4	3	2	1	-	2	-	1	3	1
5	3	2	1	-	2	-	1	3	1

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. VLSI & ES**						
Semester	**III**	Course Category Code: **PE**			End Semester Exam Type: **TE**			
Course Code	**P23VEE316**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**CAD for VLSI Circuits**	**3**	**-**	**-**	**3**	**40**	**60**	**100**

	On completion of the course, the students will be able to		BT Mapping (Highest Level)
Course Outcome	**CO1**	Knowledge On VLSI Design Methodologies & CAD Tools.	**K3**
	CO2	Analyze The Design Trade Off In Various Partitioning And Placement In VLSI Design Automation.	**K2**
	CO3	Solve The Performance Issues In Circuit Layout.	**K3**
	CO4	Analyze The Problem Formulations For Clock-Tree And Timing Performance Constraints	**K3**
	CO5	Demonstrate Different Levels Of Simulation And Synthesis In VLSI Circuits	**K4**

Unit-I	**VLSI Design Methodologies And Algorithms**	**Periods:9**
VLSI Design Problem, Design Domain, methods and Technologies Algorithmic and System Design, Terminology of Graph Theory, Computational Complexity, Graph Algorithms, Tractable and Intractable problems, back tracking and Branch and Bound, local Search, , Tabu Search, Genetic Algorithms.		**CO1**
Unit-II	**Partitioning & Placement**	**Periods:9**
Partitioning – Terminology ,Optimization goal ,Partitioning Algorithms- Kernighan-Lin (KL) Algorithm, Extensions of the Kernighan-Lin Algorithm, Fiduccia-Mattheyses (FM) Algorithm, Goldberg and Burstein algorithm. Placement –Optimization Objectives- Global Placement, Min-Cut Placement, Analytic Placement, Simulated Annealing, Modern Placement Algorithms, Legalization and Detailed Placement.		**CO2**
Unit-III	**Routing**	**Periods:9**
Terminology and Definitions - Single-Net Routing - Full-Netlist Routing - Horizontal and Vertical Constraint Graphs - Channel Routing Algorithms - Switchbox Routing - Over-the-Cell Routing Algorithms. Net Ordering in Area Routing.		**CO3**
Unit-IV	**Trees And Timing Closure**	**Periods:9**
Steiner Trees, Maze Search - Basic Concepts in Clock Networks, Problem Formulations for Clock-Tree Routing - Modern Clock Tree Synthesis, Zero Global Skew, Clock Tree Buffering. Timing Analysis and Performance Constraints - Timing-Driven Placement - Timing-Driven Routing, The Bounded-Radius, Bounded-Cost Algorithm, Prim-Dijkstra Tradeoff - Physical Synthesis, Gate Sizing, Buffering, Netlist Restructuring - Performance-Driven Design Flow.		**CO4**
Unit-V	**Instructional Activities**	**Periods:9**
Simulation – Gate level modeling – Switch level modeling- Combinational Logic Synthesis -Two level logic Synthesis.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu “VLSI Physical Design: From Graph Partitioning to Timing Closure”, 2022.
2. Sahib H.Gerez, “Algorithms for VLSI design automation”, John Wiley & Sons John Wiley & Sons, 2006.
3. Naveed A. Sherwani “Algorithm for VLSI Physical Design Automation”, 3rd Edition, Springer, 2012.Sung Kyu Lim, “Practical Problems in VLSI Physical Design Automation”, Springer, 2008.
4. ChristophnMeinel& Thorsten Theobold, “Algorithm and Data Structures for VLSI Design”,1st Edition, Kluwer Academic Publisher, 2002.

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1. https://www.ifte.de/books/eda
2. https://vast.cs.ucla.edu/software
3. https://www.scribd.com/doc/154485696/CAD-for-VLSI-Algorithms-for-VLSI-Design-Automation-by-Gerez
4. https://archive.nptel.ac.in/courses/106/106/106106088/

* TE – Theory Exam, LE – Lab Exam

Dr. P. Raja, Chairman - Bos

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	2	2	3	-	1	2	-	1
2	2	2	2	3	-	1	2	-	1
3	2	2	2	3	-	1	2	-	1
4	2	2	2	3	-	1	2	-	1
5	2	2	2	3	2	1	2	2	1

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: **M.Tech. VLSI & ES**						
Semester	III	Course Category Code: **PE**			End Semester Exam Type: **TE**			
Course Code	P23VEE317	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Advanced Image Processing**	**3**	**-**	**-**	**3**	**40**	**60**	**100**

Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Understand advanced concepts and techniques in image processing.	**K2**
	CO2	Apply advanced image processing algorithms for image enhancement, segmentation, and feature extraction.	**K3**
	CO3	Analyze and evaluate various image transform techniques for image analysis.	**K2**
	CO4	Design and implement deep learning-based approaches for image analysis tasks.	**K4**
	CO5	Apply state-of-the-art image processing algorithms and tools to solve complex problems	**K3**

UNIT-I	**Digital Image Fundamentals**	**Periods:9**
Representation of Image, pixels, Fundamentals in digital image processing, Application of digital image processing system, Elements of Digital Image, Processing systems, Structure of the Human, Image Formation in the Eye, Image Sampling and Image Quantization, Introduction to Tools used in Image processing.		**CO1**
UNIT-II	**Image Enhancement and Restoration**	**Periods:9**
Gray level transformations, Histogram Modification Techniques – Image Smoothening – Image Sharpening – Spatial Filtering – Frequency Domain Filtering. Image Degradation/Restoration Process model, Nosie models, its restoration and periodic Nosie reduction, Linear, Position-Invariant Degradation, Filtering and its types,		**CO2**
UNIT-III	**Image Segmentation and Recognition**	**Periods:9**
Detection of Discontinuities – Edge Linking and Boundary Detection – Thresholding – Region Based Segmentation – Morphology operations. Pattern classification - Clustering and Matching - Knowledge representation and use for scene analysis and image understanding (2D and 3D) - Object recognition and identification – Applications.		**CO3**
UNIT-IV	**Pattern Recognition**	**Periods:9**
Patterns and Pattern classes – Decision Theoretic Methods – Matching - Statistical (Parametric) Decision making – Optimum Statistical Classifiers – 2-D & n-D Decision boundaries – Distance Measures, Non-Parametric decision making: Single & K- Nearest neighbor classification – Adaptive decision boundaries – Adaptive discriminant functions – SVM classification – Clustering: Hierarchical clustering – Partitional clustering - K means Algorithm – Iso data algorithm.		**CO4**
UNIT-V	**Instructional Activities**	**Periods:9**
Simulation on Image Enhancement, Segmentation, Image Restoration and perform histogram equalization using MATLAB tool.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. "Digital Image Processing" By Rafael C. Gonzalez And Richard E. Woods, 4th Edition, Pearson Education, USA., 2018.
2. "Deep Learning" By Ian Goodfellow, Yoshua Bengio, Aaron Courville, MIT Press, 2016.
3. Anil K. Jain, Fundamentals Of Digital Image Processing, 1st Edition, Pearson India, 2015.
4. Ian Goodfellow, Yoshua Bengio, Aaron Courville, "Deep Learning," MIT Press, 2016.

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1. https://nptel.ac.in/courses/117/105/117105079/
2. https://staff.fnwi.uva.nl/r.vandenboomgaard/IPCV20172018/LectureNotes/index.html
3. http://www.vssut.ac.in/lecture_notes/lecture1423722885.pdf
4. https://shodhganga.inflibnet.ac.in/bitstream/10603/152244/8/08_chapter%201.pd

* TE – Theory Exam, LE – Lab Exam

Dr. P. Raja, Chairman - Bos

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	3	-	2	2	-	-	1	-	2
2	3	-	2	2	-	-	1	-	2
3	3	-	2	2	-	-	1	-	2
4	3	-	2	2	-	-	1	-	2
5	3	-	2	2	3	-	1	3	2

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: M.Tech VLSI & ES						
Semester	III	Course Category Code: PE				End Semester Exam Type: ES		
Course Code	P23VEE318	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	Hardware Software Co-Design	3	0	0	3	40	60	100

Course Outcome	On completion of the course, the students will be able to	BT Mapping (Highest Level)
CO1	Understand Hardware software synthesis algorithms.	K2
CO2	Synthesize System Communication infrastructure	K3
CO3	Design the compiler development environment	K3
CO4	To optimize Hardware and Software Code design	K2
CO5	Implement the cosyma system and lycos system.	K4

UNIT-I	Co- Design Models:	Periods: 9
Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.Concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification		CO1
UNIT-II	**Prototyping And Emulation:**	**Periods: 9**
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure. Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems, Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.		CO2
UNIT-III	**Compilation Techniques**	**Periods: 9**
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.		CO3
UNIT-IV	**Synthesis And Optimization**	**Periods: 9**
Unified hardware/software representations, Hardware/software partitioning techniques, Hardware/software synthesis methodologies. Current hardware/software code sign research. Optimization algorithms for hardware/software code sign.		CO4
UNIT-V	**Instructional Activities**	**Periods: 9**
Simulation – Design representation for system level synthesis, system level specification languages, Languages for System, Design-II: Heterogeneous specifications and multi-language co-simulation.		CO5

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Books

1. Jorgen Staunstrup, Wayne Wolf, “Hardware / Software Co- Design Principles And Practice”,Springer, 2009.
2. Kluwer, “Hardware / Software Co- Design Principles And Practice”, Academic Publishers,2002.
3. M.J.S.Smith, “Application-Specific Integrated Circuits”,(1997). Addison Wesley.
4. Soonhoi Ha, Jürgen Teich, Handbook Of Hardware/Software Codesign”, Springer, 2017.

Web References

1. https://nptel.ac.in/courses/106105159
2. https://www.cs.ccu.edu.tw/~pahsiung/courses/soc/notes/SoC_Design_Flow_Tools_Codesign.pdf
3. https://archive.nptel.ac.in/courses/106/103/106103182/
4. https://archive.nptel.ac.in/content/storage2/courses/108105057/Pdf/Lesson-1.pdf

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	2	1	2	-	1	3	3	-
2	2	2	1	2	-	1	3	3	-
3	2	2	1	2	-	1	3	3	-
4	2	2	1	2	-	1	3	3	-
5	2	2	1	2	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: **M.Tech. - VLSI & ES**						
Semester	**III**	Course Category Code: **PE**				End Semester Exam Type: **TE**		
Course Code	**P23VEE319**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Micro Electro Mechanical Systems**	**3**	**0**	**0**	**3**	**40**	**60**	**100**

Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Understand the fabrication techniques in MEMS technology.	**K2**
	CO2 Find suitable applications of MEMS sensors and actuators working based on the applications	**K3**
	CO3 Express the different fabrication methods used of MEMS technology.	**K2**
	CO4 Apply knowledge and use design tools with appropriate skill	**K2**
	CO5 Solve the integration issues in mechanical and electrical micro system components.	**K4**

UNIT-I	**Micro fabrication**	**Periods: 9**
Silicon based MEMS processes – New Materials – Review of Electrical and Mechanical concepts in MEMS – Semiconductor devices – Stress and strain analysis– Flexural beam bending- Torsional deflection.		**CO1**
UNIT-II	**Sensors And Actuators**	**Periods: 9**
Electrostatic sensors – Parallel plate capacitors – Applications – Inter digitated Finger capacitor – Comb drive devices – Thermal Sensing and Actuation – Thermal expansion – Thermal couples – Thermal resistors – Applications – Magnetic Actuators – Micro magnetic components. Piezoresistive sensors – Piezoresistive sensor materials - Stress analysis of mechanical elements –Applications to Inertia, Tactile and Flow sensors		**CO2**
UNIT-III	**Micromachining**	**Periods: 9**
Silicon Anisotropic Etching – Anisotrophic Wet Etching – Dry Etching of Silicon – Plasma Etching – Deep Reaction Ion Etching (DRIE) – Isotropic Wet Etching – Gas Phase Etchants – Case studies – Basic surface micromachining processes – Structural and Sacrificial Materials – Acceleration of sacrificial Etch – Striction and Antistriction methods – Assembly of 3D MEMS – Foundry process.		**CO3**
UNIT-IV	**Polymer And Optical MEMS:**	**Periods: 9**
Polymers in MEMS– Polimide - SU-8 - Liquid Crystal Polymer (LCP) – PDMS – PMMA – Parylene – Fluorocarbon - Application to Acceleration, Pressure, Flow and Tactile sensors- Optical MEMS – Lenses and Mirrors – Actuators for Active Optical MEMS.		**CO4**
UNIT-V	**Instructional Activities**	**Periods: 9**
Implement Micro machined antennas. Micro strip antennas – design parameters. Micromachining to improve performance. Reconfigurable antennas.		**CO5**

Lecture Periods:45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods:45**

Reference Books

1. Chang Liu, 'Foundations of MEMS', Pearson Education Inc., 2006.
2. Varadan, V. K., Jose, K. A., Vinoy, Kalarickaparambil Joseph, "RF MEMS and their Applications", Chichester,
3. England ; Hoboken, NJ : John Wiley, 2014.
4. Dirk Zielke Microsystems: Micro-Electro-Mechanical Systems, CreateSpace Independent Publishing Platform, 2016

Web References

1. https://www.google.co.in/books/edition/_/8DhlNx5IkNAC?hl=en&gbpv=
2. https://www.google.com/search?tbm=bks&q=Chang+Liu%2C+%E2%80%98Foundations+of+MEMS%E2%80%99%2C+Pearson+Education+Inc.%2C+2006
3. https://www.google.co.in/books/edition/Radio_Frequency_Micromachined_Switches_S/e1OWDwAAQBAJ?hl=en&gbpv=1&dq=G.M.Rebeizhttps://books.google.co.in/books?id=g0v3r6WNaBkC&printsec=frontcover&dq=Mohamed+Gad-el-,+editor

4. https://books.google.co.in/books?id=20j7IaDKlOUC&printsec

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	1	-	2	2	-	-	1	3	3
2	1	-	2	2	-	-	1	3	3
3	1	-	2	2	-	-	1	3	3
4	1	-	2	2	-	-	1	3	3
5	1	-	2	2	3	-	1	3	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

PROFESSIONAL ELECTIVE COURSES		
Professional Elective–VI (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEE320	Smart Technologies for Pervasive Computing
2	P23VEE321	Robotics and Automation
3	P23VEE322	Semiconductor Devices and Modeling
4	P23VEE323	VLSI for Wireless Communication
5	P23VEE324	RISC Processor Architecture and Programming

Department	**Electronics and Communication Engineering**	Programme: **M.Tech. VLSI & ES**						
Semester	**III**	Course Category Code: **PE**				End Semester Exam Type: **TE**		
Course Code	**P23VEE320**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Smart Technologies for Pervasive Computing**	**3**	**0**	**0**	**3**	**40**	**60**	**100**

Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Narrate different modulation schemes and communication concepts	**K2**
	CO2	Demonstrate the Transmitter Architecture for wireless communication	**K3**
	CO3	Interpret about Receiver Architecture and low noise amplifier design	**K3**
	CO4	Design of Phase/Frequency Processing Components	**K2**
	CO5	Simulation of VLSI Circuit design using various simulation tools	**K5**

UNIT-I	**Modulation Schemes**	**Periods: 9**
Review of modulation schemes- BASK-QPSK-OQPSK- Classical Channel-Additive White Gaussian noise-Wireless Channet-Multi path Fading-Review of spread spectrum & its types-Performance in the presence of noise-narrow and wide-band interference - Impedance Matching		**CO1**
UNIT -II	**Transmitter Architecture**	**Periods: 9**
Transmitter back end- design philosophy –Direct Conversion- Quadrature LO generator- single ended RC- single ended LC- RC with differential stages- divider based generator, power amplifier design-power output control, Class A, AB/B/C/E amplifiers.		**CO2**
UNIT-III	**Receiver Architecture**	**Periods: 9**
Receiver Front End - Heterodyne architectures - Filter Design - low noise amplifier- wideband LNA design, narrow band LNA impedance matching- core amplifier- Qualitative Description of the Gilbert Mixer.		**CO3**
UNIT-IV	**Phase/Frequency Processing Components**	**Periods: 9**
PLL-based frequency synthesizer- phase detector- dividers- Oscillators- Loop filter- first-order, second order- higher order filters- design approaches- DECT Application.		**CO4**
UNIT-V	**Instructional Activities**	**Periods: 9**
Simulation of modulation schemes in AWGN channel, Basic FHSS and DSSS, Transmitter design using direct conversion, LNA Implementation		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Reference Books

1. Bosco Leung, "VLSI for wireless Communication", Springer, 2nd Edition, 2011.
2. Andreas F.Molisch, "Wideband wireless Digital Communication", Prentice Hall PTR, 2001.
3. BehzadRazavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 2016.
4. Xiaodong Wang and H. Vincent Poor, "Wireless Communication System Advanced Techniques for Signal Reception, Pearson Education. 2004.

Web References

1. https://archive.nptel.ac.in/courses/117/102/117102062/
2. https://nptel.ac.in/courses/106/106/106106167/
3. www.aticourses.com/Advanced%20Topics%20in%20Digital%20Signals
4. www.nptelvideos.in/2012/12/wireless-communication.html

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	1	1	3	3	-
2	2	-	3	3	1	1	3	3	-
3	2	-	3	3	1	1	3	3	-
4	2	-	3	3	1	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: M.Tech VLSI & ES						
Semester	III	Course Category Code: PE			End Semester Exam Type: TE			
Course Code	P23VEE321	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	Robotics And Automation	3	0	0	3	40	60	100

Course Outcome	On completion of the course, the students will be able to		BT Mapping (Highest Level)
	CO1	Explain the fundamentals of robotics and its components.	K2
	CO2	Ability to apply spatial transformation to obtain forward kinematics equation of robot manipulators.	K3
	CO3	Demonstrate an ability to generate joint trajectory for motion planning	K3
	CO4	Understand the application of Robots and its operations.	K2
	CO5	Develop simple robot control systems integrating perception, planning, and action.	K4

UNIT-I	Robot Mechanical Structure	Periods: 9
Classification-History - Robots components-Degrees of freedom-Robot joints- coordinates - Reference frames-workspace - actuators-sensors- Position, velocity and acceleration sensors-Torque sensors-tactile and touch sensors-proximity and range sensors- vision system-social issues.		CO1
UNIT-II	**Robot Arm Kinematics**	**Periods: 9**
Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.		CO2
UNIT-III	**Robot Arm Dynamics**	**Periods: 9**
Lagrange - Euler formulation, joint velocities - kinetic energy - potential energy and motion equations - generalized D'Alembert equations of motion.		CO3
UNIT-IV	**Robot Applications**	**Periods: 9**
Material Transfer & Machine Loading / Unloading - General Consideration in robot material handling transfer applications - Machine loading and unloading. Processing Operations: Spot welding - Continuous arc welding - spray coating - other processing operations using robots.		CO4
UNIT-V	**Instructional Activities**	**Periods: 9**
Design and develop robotic arm, Line follower models, Mobile Robo and Aerial robot, Robotics simulation with Webots.		CO5

Lecture Periods:45	Tutorial Periods: -	Practical Periods: -	Total Periods:45

Reference Books

1. R.K. Mittal and I J Nagrath, "Robotics and Control", Tata Mac Graw Hill, Fourth Reprint 2003.
2. Saeed B. Niku,"Introduction to Robotics", Pearson Education, 2002.
3. S.R. Deb, "Robotics Technology and flexible automation", Tata McGraw-Hill Education., 2009.
4. Richard D. Klafter, Thomas .A, ChriElewski, Michael Negin, "Robotics Engineering an Integrated Approach", PHI Learning. 2009.

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1. http://www.nptel.iitm.ac.in
2. http://www.ocw.mit.edu
3. https://www.edx.org/learn/robotic-process-automation
4. https://www.iare.ac.in/sites/default/files/lecture_notes/ROBOTICS_LECURE_NOTES

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	1	1	3	-	3
2	2	-	3	3	1	1	3	-	3
3	2	-	3	3	1	1	3	-	3
4	2	-	3	3	1	1	3	-	3
5	2	2	3	3	2	1	3	-	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: M.Tech VLSI & ES						
Semester	III	Course Category Code: PE				End Semester Exam Type: TE		
Course Code	P23VEE322	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	Semiconductor devices and Modeling	3	0	0	3	40	60	100

Course Outcome	On completion of the course, the students will be able to		BT Mapping (Highest Level)
	CO1	Describe the various Transport in Semiconductor and their impact on performance of the device.	K3
	CO2	Analyze the various characteristics of Junction Devices	K2
	CO3	Analyze the BJT at High Frequencies	K3
	CO4	Discuss the device level characteristics of FET Transistor.	K2
	CO5	Understanding the Modelling of semiconductor devices	K3

UNIT-I	Charge Transport in Semiconductors	Periods: 9
Semiconductor Materials, Carrier Concentration, Carrier Drift, Carrier Diffusion, Hall effect, Current Density Equations, Einstein's relation Connecting μ and D, Generation and Recombination Process, Continuity Equation, Thermionic Emission, Tunnelling, Ballistic Transport, High Field Effects.		CO1
UNIT-II	**Junction Devices**	**Periods: 9**
pn junction under Thermal Equilibrium, PN junction under applied Bias, Static Current - Voltage Characteristics of PN junctions, Transient analysis, Applications - Voltage Regulator, Variable Capacitor, Tunnel Diode.		CO2
UNIT-III	**Bipolar Devices**	**Periods: 9**
Basic BJT Parameters- Ebers Moll Model, Operation of the BJT at High Frequencies- Small Signal Equivalent Circuit, Design of High Frequency Transistors- Second order Effects - Nonconventional - Polysilicon Emitter Transistor- Heterojunction Bipolar Transistors.		CO3
UNIT-IV	**Field-Effect Transistors**	**Periods: 9**
Field Effect Transistors (JFET, MESFET, HEMT), MOS Band diagram and C-V characteristics, Threshold voltage and Interface charges, MOSFET I-V, gradual channel approximation and frequency response, non-idealities and CMOS		CO4
UNIT-V	**Instructional Activities**	**Periods: 9**
Simulation a models for Semiconductor Devices: MOSFET, PN diode and BJT		CO5

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Books

1. Nandita DasGupta and Amitava DasGupta, " Semiconductor Device Modeling and Technology ", Prentice-Hall of India Pvt. Ltd, 2004
2. P. Bhattacharya, Semiconductor Optoelectronics Devices, 2nd Edition, PHI, 2009.
3. J P Collinge, C A Collinge, "Physics of Semiconductor devices" Springer, 2002.
4. S.M.Sze, Kwok.K. NG, "Physics of Semiconductor devices", Springer, 2006.

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2. https://www.phindia.com/Books/BookDetail/9788120323988/semiconductor-devices-dasgupta-dasgupta
3. https://www.comsol.com/support/learning-center/article/Introduction-to-Simulating-Semiconductor-Devices-50011
4. https://books.google.co.in/books/about/SEMICONDUCTOR_DEVICES.html?id=PlaC-M50GTUC&redir_esc=y

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	1	-	-	-	-	3	-	3
2	1	-	2	-	-	-	3	-	3
3	2	-	1	-	-	-	3	-	3
4	-	-	-	-	1	-	3	-	3
5	2	-	2	1	1	-	3	-	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	Electronics and Communication Engineering	Programme: M.Tech VLSI & ES						
Semester	III	Course Category Code: PE				End Semester Exam Type: TE		
Course Code	P20VEE323	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	VLSI for Wireless Communication	3	0	0	3	40	60	100

Course Outcome	On completion of the course, the students will be able to	BT Mapping (Highest Level)
	CO1 Narrate different modulation techniques and its components for transmission	K2
	CO2 Demonstrate the receiver Architecture for wireless communication	K3
	CO3 Interpret the concepts of low noise Amplifiers & mixers	K3
	CO4 Explain the concepts of Analog to digital Converters & mixers	K2
	CO5 Understand the concepts of the VLSI Architecture for wireless Communication	K5

UNIT-I	Introduction	Periods: 9
Review of modulation schemes- BASK-QPSK-OQPSK- Classical Channel-Additive White Gaussian noise-Wireless Channel-Path Environment-Multi path Fading-Review of spread spectrum & its types-Performance in the presence of noise-narrow and wide-band interference - Impedance Matching		CO1
UNIT-II	**Receiver Architecture**	**Periods: 9**
Receiver Front End - General Design Philosophy- Heterodyne architectures - Filter Design - Band Selection Filter - Image Rejection Filter - Channel Filter - Non idealities and Design Parameters - Harmonic Distortion - Inter-modulation - Cascaded Nonlinear Stages - Gain Compression - Blocking - Noise Figure - Design of Front end parameter for DECT		CO2
UNIT-III	**Low Noise Amplifiers & Mixers**	**Periods: 9**
Low Noise Amplifier - Matching for Noise and Stability - Matching for Power - Wideband LNA Design - Narrowband LNA - Salient features of LNA -Core Amplifier Design Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain - Distortion - Switching Mixer- Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Sampling Mixer		CO3
UNIT-IV	**Analog to Digital Converters & Synthesizer**	**Periods: 9**
Delta Modulators - Low Pass Sigma Delta Modulators - High Order Modulators - One Bit DAC and ADC -Passive Low Pass Sigma Delta Modulator - Band pass Sigma Delta Modulators - PLL based Frequency Synthesizer- Voltage Controlled Oscillators - Phase Detector - Analog Phase Detectors - Digital Phase Detectors.		CO4
UNIT-V	**Instructional Activities**	**Periods: 9**
Implementations: VLSI architecture for Multi-tier Wireless System - Hardware Design Issues for a Next generation CDMA System - Efficient VLSI Architecture for Base Band Signal processing - Frequency Synthesizers using the appropriate simulation tool		CO5

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Reference Book

1. Bosco Leung, "VLSI for wireless Communication", Springer, 2nd Edition, 2011.
2. Andreas F.Molisch, "Wideband wireless Digital Communication", Prentice Hall PTR, 2001.
3. BehzadRazavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 2016.
4. Xiaodong Wang and H. Vincent Poor, "Wireless Communication System Advanced Techniques for Signal Reception, Pearson Education. 2004.

Web References

1. https://archive.nptel.ac.in/courses/117/102/117102062/

2. https://nptel.ac.in/courses/106/106/106106167/
3. www.aticourses.com/Advanced%20Topics%20in%20Digital%20Signals
4. www.nptelvideos.in/2012/12/wireless-communication.html

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

Cos	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	1	1	3	3	-
2	2	-	3	3	1	1	3	3	-
3	2	-	3	3	1	1	3	3	-
4	2	-	3	3	1	1	3	3	-
5	2	2	3	3	2	1	3	3	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme: M.Tech **VLSI & ES**						
Semester	**III**	Course Category Code: **PE**				End Semester Exam Type: **TE**		
Course Code	**P23VEE324**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**RISC Processor Architecture and Programming**	**3**	**-**	**0**	**3**	**40**	**60**	**100**

Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Describe the programmer's model of ARM Architecture and create and test assembly level programming.	**K2**
	CO2	Analyze various types of co-processors and design suitable co-processor interface to ARM processor.	**K3**
	CO3	Identify the architectural support of ARM for operating system and analyze the function of memory Management unit of ARM.	**K4**
	CO4	Students will develop more understanding on the concepts ARM Architecture, programming and application development.	**K3**
	CO5	The learning process delivers insight into various embedded processors of RISC architecture / computational processors with improved design strategies	**K4**

UNIT-I	**AVR Architecture**	**Periods:09**
Introduction to Processor Design- Processor Architecture and Organization – Instruction Set design – Processor Design Trade off-Reduced Instruction set Computer – ARM Architecture- Arcon RISC Machine– Architectural Inheritance– Core & Architectures-- The ARM Programmer's model –ARM development Tools		**CO1**
UNIT-II	**ARM Processor And Programming**	**Periods:09**
ARM Assembly Language Programming –Data Processing Instructions ,Data transfer Instructions ,Control Flow Instructions ,Writing Simple assembly Programs-ARM Organization and Implementation - 3 stage ARM pipeline Organization ,ARM Instruction Execution, ARM Implementation ,ARM Coprocessor interface		**CO2**
UNIT-III	**Memory Management**	**Periods:09**
Introduction-Memory Management -Types of memory management, Addressing Modes, Memory protection, Virtual memory, Memory Management Unit, Cache Management ,Memory Access instruction ,Memory Alignment		**CO3**
UNIT-IV	**ARM Application Development**	**Periods:09**
Introduction to RT implementation with ARM Microcontroller—Exception Handling– Interrupts– Interrupt handling schemes- Firmware and boot loader– Free RTOS Embedded Operating Systems concepts– example on ARM core like ARM9 processor		**CO4**
UNIT-V	**Instructional Activities**	**Periods:09**
Assembly programming for Arithmetic operations- Memory access and alignment in ARM- Implementation of Exception handling- Performance analysis of RISC and CISC		**CO5**

Lecture Periods: 45	**Tutorial Periods: -0**	**Practical Periods: -0**	**Lecture Periods: 45**

Reference Books

1. Steve Furber, 'ARM system on chip architecture', Addision Wesley 2009.
2. Muhammad Ali Mazidi, Sarmad Naimi ,Sepehr Naimi' AVR Microcontroller and Embedded Systems using Assembly and C", Pearson Education 2014
3. Developer's Guide Designing and Optimizing System Software', Elsevier 2007.
4. ARM Architecture Reference Manual, LPC213x User Manual.

Web References

1. WWW.Nuvoton .com/websites on Advanced ARM Cortex Processors
2. WWW.ARM7-Based Microcontrollers

3. WWW. AVR Microcontroller and Embedded Systems using Assembly and C
4. WWW. ARM Architecture

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	1	1	3	2	-	-	2	3	3
2	1	1	3	2	-	-	2	3	3
3	1	1	3	2	-	-	2	3	3
4	1	1	3	2	-	-	2	3	3
5	2	2	3	2	3	2	2	3	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**Electronics and Communication Engineering**	Programme**: M.Tech. - VLSI & ES**						
Semester	**III**	Course Category: **PA**			End Semester Exam Type: **LE**			
Course Code	**P23VEW301**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Title	**Project Phase - I**	**-**	**-**	**12**	**6**	**50**	**50**	**100**

Aim & Objective:

The project work aims to develop the work practice and to apply theoretical and practical tools/techniques for solving real life problems related to industry and current research. The objective of the project work is to improve the professional competency and research attitude by touching the areas which are not covered in theory or laboratory classes.

- The project work shall be a design project/experimental project and/or computer simulation project on any of the topic in Electronics and Communication Engineering or related field.
- The project work shall be allotted individually on different topics.
- The students shall be encouraged to do their project work in the parent institute itself. In exceptional cases the students shall be permitted to undertake continue their project outside the parent institute with appropriate permission from Head of the institution through the Project Coordinator.
- Department shall constitute an Evaluation Committee to review the project work.
- The Evaluation committee shall consist of at least three faculty members namely internal guide, project coordinator and another expert in the specified area of the project.

The student is required to undertake the project phase I during the third semester and the same shall be continued in the 4^{th} semester (Phase II). Phase I consist of preliminary thesis work, three reviews of the work and the submission of preliminary report. First review shall highlight the topic, objectives and origin of problem, second review shall highlight, Literature survey, methodology and expected results. Third review shall evaluate the progress of the work, preliminary report and scope of the work which shall be completed in the 4thsemester. Also, the evaluation of project phase - I shall be done externally.

Department	**Electronics and Communication Engineering**	Programme**: M.Tech. - VLSI & ES**						
Semester	**III**	Course Category: **PA**			End Semester Exam Type: **-**			
Course Code	**P23VEW302**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Title	**Internship**	-	-	-	2	100	-	100

Students should undergo training or internship during summer / winter vacation at Industry/ Research organization / University (after due approval from the Programme Academic Coordinator and Department Consultative Committee (DCC). In such cases, the internship/training should be undergone continuously (without break) in one organization. Normally no extension of time is allowed. However, DCC may provide relaxation based on the exceptional case. The students can undergo three to four weeks of internship in established industry / Esteemed institution during vacation period. The student should give presentation and send report to DCC. The Internship is assessed internally for 100 marks.

Department	**Electronics and Communication Engineering**	Programme**: M.Tech. - VLSI & ES**						
Semester	**III**	Course Category: **AEC**			End Semester Exam Type: **-**			
Course Code	**P23VEC301**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Title	**NPTEL/SWAYAM/MOOC**	-	-	-	2	100	-	100

Student should register online courses like MOOC / SWAYAM / NPTEL etc. approved by the Department committee comprising of HoD, Programme Academic Coordinator and Subject Experts. Students have to complete relevant online courses successfully. The list of online courses is to be approved by Academic Council on the recommendation of HoD at the beginning of the semester, if necessary, subject to ratification in the next Academic council meeting. The Committee will check the progress of the student and recommend the grade (100% Continuous Assessment pattern) based on the marks secured in online examinations. The marks attained for this course is not considered for CGPA calculation**.**

SEMESTER – IV

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Project Work										
1	P23VEW403	Project Phase - II	PA	0	0	24	12	50	50	100
Total							**12**	**50**	**50**	**100**

Department	Electronics and Communication Engineering	Programme: M.Tech(VLSI & ES)						
Semester	IV	Course Category: PA			*End Semester Exam Type: LE			
Course Code	P23VEW403	Periods / Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	Project Phase - II	-	-	24	12	50	50	100

Aim & Objective:

The project work aims to develop the work practice and to apply theoretical and practical tools/techniques for solving real life problems related to industry and current research. The objective of the project work is to improve the professional competency and research attitude by touching the areas which are not covered in theory or laboratory classes.

- The project work shall be a design project/experimental project and/or computer simulation project on any of the topic in Electronics and Communication Engineering or related field.
- The project work shall be allotted individually on different topics.
- The students shall be encouraged to do their project work in the parent institute itself. In exceptional cases the students shall be permitted to undertake continue their project outside the parent institute with appropriate permission from Head of the institution through the Project Coordinator.
- Department shall constitute an Evaluation Committee to review the project work.
- The Evaluation committee shall consist of at least three faculty members namely internal guide, project coordinator and another expert in the specified area of the project.

The student is required to undertake the project phase I during the third semester and the same shall be continued in the 4th semester (Phase II). Phase I consist of preliminary thesis work, three reviews of the work and the submission of preliminary report. First review shall highlight the topic, objectives and origin of problem, second review shall highlight, Literature survey, methodology and expected results. Third review shall evaluate the progress of the work, preliminary report and scope of the work which shall be completed in the 4thsemester. Also, the evaluation of project phase - I shall be done externally