SRI MANAKULA VINAYAGAR
ENGINEERING COLLEGE
(An Autonomous Institution)

Puducherry

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

M.TECH.
VLSI AND EMBEDDED SYSTEMS
(REGULATIONS - 2020)

CURRICULUM AND SYLLABI

Board Chairman - ECE

VISION AND MISSION OF THE INSTITUTE

Vision

To be globally recognized for excellence in quality education, innovation and research for the transformation of lives to serve the society

Mission

M1 - Quality Education	To provide comprehensive academic system that amalgamates the cutting-edge technologies with best practices.
M2 - Research **and Innovation**	To foster value-based research and innovation in collaboration with industries and institutions globally for creating intellectuals with new avenues.
M3 - Employability and Entrepreneurship	To inculcate the employability and entrepreneurial skills through value and skill-based training
M4: - Ethical values	To instill deep sense of human values by blending societal righteousness with academic professionalism for growth of society

VISION AND MISSION OF THE DEPARTMENT

Vision

Facilitate academic excellence and research among Electronics and Communication Engineers to meet the global needs with high competence and ethical professionalism

Mission

M1 - Academic Excellence	To impart learning skills to meet the global challenges in the field of Electronics and Communication Engineering
M2 - Research and Innovation	To provide excellence in research and innovation through multidisciplinary specialization
M3 - Employability and Entrepreneurship	To enhance inter and intrapersonal skills among students to make them employable and entrepreneurs
M4 - Ethics	To inculcate the significance of human values and professional skills to serve the society

PROGRAMME OUTCOMES (POs)

PO1: Exploration of Research: An ability to independently carry out research/investigation and development work to solve practical problems.

PO2: Technical Skill: An ability to write and present a substantial technical report/document.

PO3: Expertise in Academics: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Scholarship of Knowledge: Acquire in-depth knowledge of specific discipline or professional area, including wider and global perspective, with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge, and integration of the same for enhancement of knowledge.

PO5: Usage of Modern Tools: Create, select, learn and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex engineering activities with an understanding of the limitations.

PO6: Ethical Practices and Social Responsibility: Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Technical Knowledge	To Provide a solid basis and experience in the field of VLSI and Embedded System to meet the unique needs of the society
PEO2: Leadership Skill	To develop good leadership skills in the respective domain to perform creative and collaborative work
PEO3: Research and Development	To inculcate practical knowledge to undertake quality interdisciplinary research projects addressing industrial and social needs
PEO4: Professional Behavior	To train students to be an active collaborators and responsible engineers to solve social, technical and engineering challenges.

PROGRAM SPECIFIC OUTCOMES (PSOs)

.**PSO1-Technical Knowledge in VLSI and Embedded Systems**	Ability to apply cutting-edge technology to solve complex problems and provide an optimized solution in the domain of VLSI and Embedded Systems.
PSO2- Competency in VLSI Design	Ability to design and test systems by applying the concepts of FPGA, ASIC, System on Chip etc.
PSO3-Competency in Embedded System	Ability to develop and analyze Embedded Systems to solve real time societal problems.

CURRICULUM

SEMESTER – I										
Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P20BST106	Applied Mathematics	BS	2	2	0	3	40	60	100
2	P20VET101	Digital System Design using VHDL	PC	3	0	0	3	40	60	100
3	P20VET102	VLSI Design Techniques	PC	3	0	0	3	40	60	100
4	P20VET103	FPGA Based System Design	PC	3	0	0	3	40	60	100
5	P20CCT101	Research Methodology and IPR	PC	2	0	0	2	40	60	100
6	P20VEE1XX	Professional Elective-I	PE	3	0	0	3	40	60	100
Practical										
7	P20VEP101	VLSI Design Laboratory	PC	0	0	4	2	50	50	100
8	P20CCP101	Technical Report Writing and Seminar	PC	0	0	4	2	100	-	100
Audit Course										
9	P20ACT10X	Audit Course-I	AC	0	0	2	-	100	-	100
Employability Enhancement Course										
10	P20VEC1XX	Employability Enhancement Course-I	EEC	0	0	4	-	100	-	100
Total							**21**	**590**	**410**	**1000**

SEMESTER – II										
Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P20VET204	Advanced Digital System Design	PC	3	0	0	3	40	60	100
2	P20VET205	Embedded Networking	PC	3	0	0	3	40	60	100
3	P20VET206	Embedded System Design	PC	3	0	0	3	40	60	100
4	P20VET207	Low Power Digital VLSI Design	PC	3	0	0	3	40	60	100
5	P20VEE2XX	Professional Elective-II	PE	3	0	0	3	40	60	100
6	P20VEE2XX	Professional Elective-III	PE	3	0	0	3	40	60	100
Practical										
7	P20VEP202	Embedded System Design Laboratory	PC	0	0	4	2	50	50	100
8	P20CCP202	Seminar on ICT a hands-on approach	PC	0	0	4	2	100	-	100
Audit Course										
9	P20ACT20X	Audit Course-II	AC	-	-	2	-	100	-	100
Employability Enhancement Course										
10	P20VEC2XX	Employability Enhancement Course-II	EEC	-	-	4	-	100	-	100
Total							**22**	**590**	**410**	**1000**

SEMESTER – III										
Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P20VEE3XX	Professional Elective -IV	PE	3	0	0	3	40	60	100
2	P20VEE3XX	Professional Elective- V	PE	3	0	0	3	40	60	100
3	P20VEE3XX	Professional Elective- VI	PE	3	0	0	3	40	60	100
Practical										
4	P20VEW301	Project Phase-I	PW	0	0	12	6	50	50	100
5	P20VEW302	Internship	PW	0	0	0	2	100	-	100
Employability Enhancement Course										
6	P20VES301	NPTEL/ GIAN/ MOOC	EEC	0	0	0	-	100	-	100
Total							**17**	**370**	**230**	**600**

SEMESTER – IV										
Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Practical										
1	P20VEW403	Project Phase-II	PW	0	0	24	12	50	50	100
Total							**12**	**50**	**50**	**100**

BS – Basic Science
PC – Professional Core
PE – Professional Elective
PW – Project Work
CC – Common Course
AC – Audit Course
EEC – Employability Enhancement Course

Credit Distribution

Semester- I	Semester - II	Semester - III	Semester - IV	Total
21	**22**	**17**	**12**	**72**

Total number of credits required to complete
M.Tech in VLSI and Embedded Systems : 72 Credits

Annexure-I

PROFESSIONAL ELECTIVE COURSES

Sl. No.	Course Code	Course Title
Professional Elective – I		
2	P20VEE102	Advanced Microprocessor and Interfacing
3	P20VEE103	Modeling and Synthesis with Verilog HDL
4	P20VEE104	Physical Design of VLSI
5	P20VEE105	Software for Embedded System
Professional Elective – II		
1	P20VEE206	VLSI Architecture
2	P20VEE207	CAD for VLSI Circuits
3	P20VEE208	Design of Analog and Mixed VLSI Circuits
4	P20VEE209	Distributed Embedded Computing
5	P20VEE210	Internet of Things
Professional Elective – III		
1	P20VEE211	DSP Processor Architecture and Programming
2	P20VEE212	Industrial Automation using PLC and SCADA
3	P20VEE213	Principles of ASIC Design
4	P20VEE214	Real Time Systems
5	P20VEE215	Testing of VLSI Circuits
Professional Elective – IV		
1	P20VEE316	VLSI Signal Processing
2	P20VEE317	High Speed Digital Design
3	P20VEE318	Real Time Operating System
4	P20VEE319	Soft Computing
5	P20VEE320	Cloud computing and Distributed System
Professional Elective – V		
1	P20VEE321	Advanced Embedded System
2	P20VEE322	Advanced Image Processing
3	P20VEE323	Hardware Software Co-Design
4	P20VEE324	Micro-Electromechanical Systems
5	P20VEE325	Nano Electronics
Professional Elective – VI		
1	P20VEE326	Pervasive Devices and Technology
2	P20VEE327	Robotics and Automation
3	P20VEE328	System-on-Chip Design
4	P20VEE329	VLSI for Wireless Communication
5	P20VEE330	RISC Processor Architecture and Programming

Annexure-II

EMPLOYABILITY ENHANCEMENT COURSES

Sl. No.	Course Code	Course Title
1	P20ECCX01	Video & Image processing Development System
2	P20ECCX02	Android Programming
3	P20ECCX03	Artificial Intelligence and Edge Computing
4	P20ECCX04	CCNA (Routing and Switching)
5	P20ECCX05	CCNA (Wireless)
6	P20ECCX06	Cloud Computing
7	P20ECCX07	Cyber Security
8	P20ECCX08	Data Science
9	P20ECCX09	Data Science and Data Analytics
10	P20ECCX10	Data Science Using R
11	P20ECCX11	Bio signal and Image processing development system
12	P20ECCX12	Google Analytics
13	P20ECCX13	Google Cloud
14	P20ECCX14	Industry 4.0
15	P20ECCX15	Internet of Things
16	P20ECCX16	IoT using Python
17	P20ECCX17	Java Programming
18	P20ECCX18	Android Medical app development
19	P20ECCX19	Machine Learning and Deep Learning
20	P20ECCX20	Web Programming (HTML, CSS, JAVA Script)
21	P20ECCX21	Advanced Java Programming
23	P20ECCX22	Advanced Python Programming
24	P20ECCX23	Android Medical app development
25	P20ECCX24	Artificial Intelligence and Edge Computing
26	P20ECCX25	Embedded System Using Arduino
27	P20ECCX26	Embedded System Using C
28	P20ECCX27	Embedded System with IoT
29	P20ECCX28	Introduction to C Programming
30	P20ECCX29	Introduction to C++ Programming

Sl. No.	Course Code	Course Title
31	P20ECCX30	Mobile Edge Computing
32	P20ECCX31	Python Programming
33	P20ECCX32	Web Programming -I
34	P20ECCX33	Web Programming-II
35	P20ECCX34	VLSI Design
36	P20ECCX35	Machine Learning
37	P20ECCX35	Block chain
38	P20ECCX35	Speech Processing
39	P20ECCX35	Digital Signal Processing Development System
40	P20ECCX35	Data Science using Python
41	P20ECCX35	Solar and Smart Energy System with IoT
42	P20ECCX35	Fuzzy Logic and Neural Networks
43	P20ECCX35	Digital Signal Processing Development System

Annexure-III

AUDIT COURSES

Sl. No.	Course Code	Course Title
1	P20ACTX01	English for Research Paper Writing
2	P20ACTX02	Disaster Management
3	P20ACTX03	Sanskrit for Technical Knowledge
4	P20ACTX04	Value Education
5	P20ACTX05	Constitution of India
6	P20ACTX06	Pedagogy Studies
7	P20ACTX07	Stress Management by Yoga
8	P20ACTX08	Personality Development Through Life Enlightenment Skills
9	P20ACTX09	Unnat Bharat Abhiyan

SEMESTER – I

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P20BST106	Applied Mathematics	BS	2	2	0	3	40	60	100
2	P20VET101	Digital System Design using VHDL	PC	3	0	0	3	40	60	100
3	P20VET102	VLSI Design Techniques	PC	3	0	0	3	40	60	100
4	P20VET103	FPGA Based System Design	PC	3	0	0	3	40	60	100
5	P20CCT101	Research Methodology and IPR	PC	2	0	0	2	40	60	100
6	P20VEE1XX	Professional Elective-I	PE	3	0	0	3	40	60	100
Practical										
7	P20VEP101	VLSI Design Laboratory	PC	0	0	4	2	50	50	100
8	P20CCP101	Technical Report Writing and Seminar	PC	0	0	4	2	100	-	100
Audit Course										
9	P20ACT10X	Audit Course-I	AC	0	0	2	-	100	-	100
Employability Enhancement Course										
10	P20VEC1XX	Employability Enhancement Course-I	EEC	0	0	4	-	100	-	100
Total							**21**	**590**	**410**	**1000**

P20BST106	APPLIED MATHEMATICS	L	T	P	C	Hrs
		2	2	0	3	60

Course Objectives

- To learn about the core ideas in graph theory
- To understand the basic concepts of Graph algorithm which includes connectivity, paths and lattices
- To find an idea about Boolean algebra and functions with examples
- To introduce the mathematical formulation of optimization
- To solve real time problems using knowledge gained in graph algorithm and Boolean function

Course Outcomes

After completion of the course, the students will be able to

CO1 - Explain language of graphs and trees. (**K2**)
CO2 - Define and apply various algorithms in graph theory. (**K2**)
CO3 - Describe about Boolean algebra and Boolean functions(**K3**)
CO4 - Apply mathematical skills to model optimization problems. (**K3**)
CO5 - Apply graph algorithm and Boolean functions to solve real time problems. (**K3**)

UNIT –I BASICS OF GRAPH THEORY (12 Hrs)

Graphs – Data structures for graphs – Subgraphs – Operations on Graphs Connectivity – Euler, Hamilton graph and its properties- Planar graphs- Networks and the maximum flow – Minimum cut theorem - Trees – Spanning trees – Rooted trees – Matrix representation of graphs.

UNIT –II GRAPH ALGORITHM (12 Hrs)

Computer Representation of graphs – Basic graph algorithms – Minimal spanning tree algorithm – Kruskal and Prim's algorithm - Shortest path algorithms – Dijsktra's algorithm – DFS and BFS algorithms. Lattices as partially ordered sets, properties of Lattices. Lattices as Algebraic Systems, Sublattices

UNIT –III BOOLEAN ALGEBRA (12 Hrs)

Definitions and examples, Subalgebra, Direct Product and Homomorphism. Boolean Functions, Representation and Minimization of Boolean Functions, Design examples using Boolean Algebra.

UNIT –IV OPTIMIZATION TECHNIQUES (12 Hrs)

Linear Programming – Formulation of LPP – Graphical methods - Simplex method- Transportation problems- Assignment problems.

UNIT –V INSTRUCTIONAL ACTIVITY (12 Hrs)

Applications of Boolean Functions - Practical applications of Basic graph algorithms, Transportation problems and Assignment problems.

Text Books

1. Tremblley. J.P and Manohar. R, "Discrete Mathematics Structures with Application to Computer Science", Mc Graw Hill Book Company, 2017
2. Narsingh Deo, "Graph Theory: With Application to Engineering and Computer Science", PHI, 2014.
3. Kanti Swarup, Man Mohan, P.K. Gupta, "Operations Research ", Sultan Chand & Sons, 2014.

Reference Books

1. Edgar G. Goodaire & Michael M. Parameter, "Discrete Mathematics with Graph Theory", 3rd edition, Pearson Education, 2018.
2. Rao S.S, "Engineering Optimization: Theory and Practice", New Age International Pvt. Ltd., 3rd Edition, 2018.
3. Grewal B.S., "Higher Engineering Mathematics", Khanna Publishers. 34th Edition, 2005.
4. Narayanan S., Manicavachagom Pillai T.K. and Ramanaiah G., "Advanced Mathematics for Engineering Students", Vol. II S. Viswanathan & Co.
5. Venkatraman M.K., Higher Engineering Mathematics, National Publishing Co., 2000.

Web References

1. http:// www.nptel.ac.in
2. http://www.personal.psu.edu/cxg286/Math485.pdf
3. http://poincare.matf.bg.ac.rs/~zarkom/Book_Shaums_BooleanAlgebraMendelson.pdf
4. https://cds.cern.ch/record/450639/files/p60.pdf
5. https://lecturenotes.in/subject/2/applied-mathematics-1-m-1

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	-	2	-	-	1	-	-
CO2	2	-	-	2	-	-	1	-	-
CO3	2	-	-	2	-	-	1	-	-
CO4	2	-	-	2	-	-	1	-	-
CO5	2	-	-	2	2	-	1	-	-

P20VET101 DIGITAL SYSTEM DESIGN USING VHDL

L	T	P	C	Hrs
3	-	-	3	45

Course Objectives

- To expose the students in the fundamentals of combinational and sequential circuits
- To study the concepts of VHDL for digital circuits
- To implement combinational circuits using VHDL
- To understand concept of Programmable Devices, PLA, PAL, and memories
- To simulate combinational and sequential circuits using HDL

Course Outcomes

After completion of the course, the students will be able to

CO1 - Design combinational and sequential logic circuits**. (K3)**
CO2 - Describe and write VHDL coding for combinational and sequential circuit**. (K3)**
CO3 - Design the network for performing arithmetic operations**. (K3)**
CO4 - Design and implement digital system design using PLD and memories. **(K3)**
CO5 - Simulate Combinational and sequential circuits using VHDL. **(K4)**

UNIT –I DIGITAL SYSTEMS OVERVIEW (9 Hrs)

Review of combinational circuits: Adder, subtractor, code converter, decoder, encoder, Multiplexer, demultiplexer. Review of sequential circuits: Flip-flops, shift registers, synchronous counter, ripple counter, mod counter, ring counter, Johnson counter, non-sequential counters.

UNIT -II HARDWARE DESCRIPTION LANGUAGE (9 Hrs)

VHDL Description of Combinational Networks. Modelling Flip-flops using VHDL Processes. VHDL Models for a Multiplexer, Compilation and Simulation of VHDL Code, Modelling a Sequential Machine, Variables, Signals, and Constants, Arrays VHDL Operators, VHDL Functions, VHDL Procedures, Packages and Libraries.

UNIT -III DESIGN OF NETWORKS FOR ARITHMETIC OPERATIONS (9 Hrs)

Design of Parallel adder/subtractor with accumulator, serial adder with accumulator, design of binary multiplier and binary divider, signed multiplier using VHDL.

UNIT -IV DESIGNING WITH PROGRAMMABLE LOGIC DEVICES (9 Hrs)

Read Only Memories, Programmable Array Logic PALs, Programmable Logic Arrays PLAs – PLA minimization and PLA folding, Other Sequential PLDs, Design of combinational circuits using PLD's.

UNIT -V INSTRUCTIONAL ACTIVITY (9 Hrs)

Simulation of logic gates, adder, subtractor, decoder, multiplexer, flip flops, counters using VHDL.

Text Books

1. Jr.Charles H.Roth, "Fundamentals of Digital Design ", PWS Pub.Co, 7th Edition, 2014.
2. Charles H. Roth, "Digital System Design using VHDL", Thomson Learning, 3rd Edition, 2007.
3. Peter Ashenden, "Digital Design using VHDL", Elsevier, 2007.

Reference Books

1. Na Vikraman, "Advanced Digital System Design Using VHDL", Atlantic Publisher, 2020.
2. Peter Ashenden, "Digital Design using Verilog", Elsevier, 2007.
3. Clive Maxfield, "The Design Warriors's Guide to FPGAs", Elsevier, 2004.
4. John F.Wakerly, "Digital Design Principles and Practices", Prentice Hall, 4th Edition, 2001.
5. M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2000.

Web References

1. http://www2.cs.uidaho.edu/~krings/CS449
2. http://www.cs.colostate.edu/~malaiya/530/08/1Intro.pdf
3. http://www.ida.liu.se/~TDDB47/lectures/tddb47-dependability-2x3.pdf
4. https://www.tutorialspoint.com/vlsi_design/vlsi_design_vhdl_introduction.htm
5. http://www.eng.auburn.edu/~strouce/elec4200.html

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	2	-	1	3	3	-
CO2	2	-	3	2	-	1	3	3	-
CO3	2	-	3	2	-	1	3	3	-
CO4	2	-	3	2	-	1	3	3	-
CO5	2	2	3	2	2	1	3	3	-

P20VET102	VLSI DESIGN TECHNIQUES	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To learn the performance of MOS transistors
- To learn static and dynamic behaviour of CMOS design
- To understand about impact of passive components in circuits
- To implement CMOS logic in designing combinational and sequential circuits
- To learn verilog HDL programming language

Course Outcomes

After completion of the course, the students are able to

CO1 - Demonstrate the characteristics of MOS transistors with its small signal parameters. **(K3)**
CO2 - Draw stick diagram and design circuits in static and dynamic CMOS logic. **(K3)**
CO3 - Estimate the VLSI circuit performance based on resistors, inductors and capacitors. **(K3)**
CO4 - Design combinational and sequential circuits in VLSI and understand its clock distribution. **(K3)**
CO5 - Code the combinational and sequential circuits in verilog HDL language. **(K4)**

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY (9 Hrs)

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II INVERTERS AND LOGIC GATES (9 Hrs)

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics, switching times, Super buffers, Driving large capacitance loads, CMOS logic structures, Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION (9 Hrs)

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing. Scaling.

UNIT IV VLSI SYSTEM COMPONENTS, CIRCUITS AND DESIGN (9 Hrs)

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Case study on Overview of digital design with Verilog HDL for Structural, Data flow, Behavioral Styles of Hardware Description

Text Books

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2. John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley &Sons, Inc., 2002.
3. Samir Palnitkar, “Verilog HDL”, Pearson Education, 2nd Edition, 2004.

Reference Books

1. Wai Kai Chen, “VLSI Technology” CRC press, 2003.
2. J.Bhasker, B.S.Publications, “A Verilog HDL Primer”, 2nd Edition, 2001.
3. Pucknell, “Basic VLSI Design”, Prentice Hall of India Publication, 2004.
4. Wayne Wolf “Modern VLSI Design System on chip. Pearson Education.2002
5. James D Plummer, Michael D. Deal, Peter B.Griffin, “Silicon VLSI Technology: fundamentals practice and Modeling”, Prentice Hall India, 2009.

Web Reference

1. http://web.ewu.edu
2. http://ic.sjtu.edu
3. http://nptel.iitm.ac.in
4. http://ee.ncu.edu.tw/~jfli/vlsi21/lecture/ch01.pdf
5. https://www.tutorialspoint.com/vlsi_design/vlsi_design_digital_system.htm

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	3	-
CO2	2	-	3	3	-	1	3	3	-
CO3	2	-	3	3	-	1	3	3	-
CO4	2	-	3	3	-	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VET103	FPGA BASED SYSTEM DESIGN	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To recognize the basic modules of FPGA
- To explain how Technology is mapping with FPGA
- To outline routing concepts used in FPGA
- To provide the knowledge about various FPGA architectures
- To carry out the synthesis activities of various multipliers and filters

Course Outcomes

After completion of the course, the students will be able to

CO1 - Describe the various basic modules of FPGA. **(K2)**
CO2 - Relate the technology mapping with FPGA. **(K3)**
CO3 - Discuss the routing concepts of FPGA. **(K3)**
CO4 - Classify the various FPGA architectures. **(K4)**
CO5 - Synthesise various multipliers & filters. **(K4)**

UNIT I FPGA ARCHITECTURE (9 Hrs)

Introduction of basic concepts, Digital design and FPGAs. FPGA based system design, Logic blocks, Routing architecture, FPGA Fabrics, Circuit design of FPGA fabrics, Platform FPGA.

UNIT II TECNOLOGY MAPPING FOR FPGAs (9 Hrs)

Fundamental of high level synthesis, Logic synthesis, Logic optimization and technology mapping, Lookup table technology mapping, Timing analysis, Timing optimization, Area optimization

UNIT III ROUTING FOR FPGAs (9 Hrs)

Routing terminology, Strategy for routing in FPGAs, Routing for row-logic block selection, Experimental procedure Logic block architecture ,Logic block functionality vs area and efficiency, Logic block selection, Experimental procedure, Logic block area and routing model.

UNIT IV ARCHITECTURE OF FPGAs (9 Hrs)

Study of Xilinx Virtex series FPGAs, Architecture of Altera cyclone FPGA series. Comparison of Xilinx & Altera FPGAs

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Synthesis of multiplier and digital filters in FPGA and analyse the FPGA architecture and mapping of I/O pads

Text Books

1. Wayne Wolf, FPGA based system design, Prentice Hall, 2004.
2. Wayne Wolf, Modern VLSI design, System on Chip design, 3rd Ed. Prentice Hall 2002.
3. S. Trimberger, Edr, Field Programmable Gate Array technology, Kluwer Academic publication, 2009.

Reference Books

1. Ian Kuon, Russell Tessier, Jonathan Rose, FPGA Architecture, Now Publishers, 2008.
2. Scott Hauck, André Dehon, "Reconfigurable computing: the theory and practice of FPGA-based computation", Morgan Kaufmann publishers, 2008.
3. Steve Kilts*, "Advanced FPGA Design: Architecture, Implementation, and Optimization", Wiley Publisher, 2007*.
4. Pong P. Chu*, "FPGA Prototyping by VHDL / Verilog Examples "Wiley Publisher, 2008*
5. D. Pellerin and S. Thibault, Practical FPGA Programming in C, Prentice-Hall, 2005.

Web References

1. http://nptel.iitm.ac.in
2. https://dl.acm.org/doi/book/10.5555/983326
3. https://www.academia.edu/31100712/FPGA-Based_System_Design_Wayne_Wolf_SAmple_book
4. https://www.researchgate.net/publication/268424617_Design_and_Implementation_of_FPGA-Based_Systems_-A_Review
5. https://trove.nla.gov.au/work/38674264

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	3	-
CO2	2	-	3	3	-	1	3	3	-
CO3	2	-	3	3	-	1	3	3	-
CO4	2	-	3	3	-	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20CCT101	RESEARCH METHODOLOGY AND IPR	L	T	P	C	Hrs
		2	-	-	2	30

Course Objectives

- To impart knowledge and skills required for research and IPR
- Problem formulation, analysis and solutions
- Technical paper writing / presentation without violating professional ethics
- Patent drafting and filing patents

Course Outcomes

After completion of the course, the students will be able to

CO1 - Formulate research problem**. (K2)**
CO2 - Carry out research analysis. **(K2)**
CO3 - Follow research ethics. **(K2)**
CO4 - Describe today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity. **(K2)**
CO5 - Interpret IPR and filing patents in R & D. **(K3)**

UNIT I RESEARCH PROBLEM FORMULATION (6 Hrs)

Meaning of research problem- Sources of research problem, criteria characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations

UNIT II LITERATURE REVIEW (6 Hrs)

Effective literature studies approaches, analysis, plagiarism, and research ethics.

UNIT III TECHNICALWRITING /PRESENTATION (6 Hrs)

Effective technical writing, how to write report, paper, developing a research proposal, format of research proposal, a presentation and assessment by a review committee.

UNIT IV INTRODUCTION TO INTELLECTUAL PROPERTY RIGHTS (IPR) (6 Hrs)

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT V INTELLECTUAL PROPERTY RIGHTS (IPR) (6 Hrs)

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System, IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Text Books

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'" Kenwyn Publisher, 1996
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction" 2nd edition, Lansdowne publisher, 2001
3. C.R. Kothari, Gaurav Garg, New Age International, Research Methodology: Methods and Techniques 4th Edition, 2018.

Reference Books

1. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd, 2007.
2. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners" 2010.
3. C.R. Kothari, Gaurav Garg, New Age International, Research Methodology: Methods and Techniques 4th Edition, 2018.
4. Trochim, Research Methods: the concise knowledge base, Atomic Dog Publishing 2005.
5. Fink A, Conducting Research Literature Reviews: From the Internet to Paper, Sage Publications,2009.

Web References

1. https://www.scribd.com/document/427419672/Research-Methodology-and-Ipr
2. https://www.isical.ac.in/~palash/research-methodology/RM-lec9.pdf
3. https://www.wipo.int/edocs/pubdocs/en/intproperty/958/wipo_pub_958_3.pdf
4. https://lecturenotes.in/m/21513-research-methodology-
5. https://iare.ac.in/sites/default/files/MTECH-CAD.CAM-R18-RM-IP-NOTES.pdf

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	3	2	-	1	-	1	1	-	-
CO2	3	2	-	1	-	1	1	-	-
CO3	3	2	-	1	-	1	1	-	-
CO4	3	2	-	1	-	1	1	-	-
CO5	3	2	-	1	-	1	1	-	-

P20VEP101	VLSI DESIGN LABORATORY	L	T	P	C	Hrs
		-	-	4	2	30

Course Objectives

- To write code for combinational circuits in verilog HDL
- To write code for sequential circuits in verilog HDL
- To learn about SPICE tool
- To learn about FPGA interfacing
- To learn to implement VLSI circuits in FPGA
- To learn about FPGA implementation of circuits

Course Outcomes

After completion of the course, the students are able to

CO1 - Design and simulate combinational circuits in verilog HDL. **(K4)**
CO2 - Design and simulate sequential circuits in verilog HDL. **(K4)**
CO3 - Design and simulate VLSI circuits using spice tool. **(K4)**
CO4 - Interface FPGA with PC for I/O interfacing. **(K5)**
CO5 - Implement combinational and sequential circuits using FPGA/CPLD. **(K5)**

List of Experiments

1. Design and simulate combinational circuits using VHDL/Verilog HDL in Gate level, behavior level and generate test vectors
    - Adder, subtractor
    - Code converter
    - Decoder
    - Encoder
    - Multiplexer
    - Demultiplexer
    - Multiplier
    - Divider
2. Design and simulate sequencial circuits using VHDL/Verilog HDL in Gate level, behavior level and generate test vectors
    - Flip-flops
    - Shift registers (SISO, SIPO, PISO, PIPO)
    - Synchronous counter
    - Asynchronous counter
    - Mod counter
    - Sequence generator
    - Sequence detector
    - Ring and Johnson counter
3. Simulation of NMOS and CMOS circuits using SPICE.
4. FPGA/CPLD real time programming and I/O interfacing.
5. Implementation of combinational circuit in FPGA/CPLD
6. Implementation of sequential circuit in FPGA/CPLD

Reference Books

1. Jan M. Rabaey, AnanthaChandrakasan and BorivojeNikolic, “Digital Integrated Circuits - A Design Perspective “, Prentice Hall of India, 2012.
2. James D Plummer, Michael D. Deal, Peter B.Griffin, “Silicon VLSI Technology: fundamentals practice and Modeling”, Prentice Hall India, 2009.
3. Thomas, D. E., Philip.R. Moorby “The Verilog Hardware Description Language”,2nd edition, Kluwer Academic Publishers,2002.
4. Sebastian Smith, “Application Specific Integrated Circuits”, Pearson Education,2001.
5. DebaPrasad Das, VLSI Design”, Oxford University Press, 2012.

Web References

1. http://www.stem-edu.com/wp-content/uploads/2017/02/Rabaey-Digital-Integrated-Circuits-Asign Perspective-2Nd-Edition.pdf
2. http://ic.sjtu.edu
3. http://nptel.iitm.ac.in
4. http://ee.ncu.edu.tw/~jfli/vlsi21/lecture/ch01.pdf
5. https://www.tutorialspoint.com/vlsi_design/vlsi_design_digital_system.htm

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	1	3	1	-	1	3	3	-
CO2	2	1	3	1	-	1	3	3	-
CO3	2	1	3	1	-	1	3	3	-
CO4	2	1	3	1	-	1	3	3	-
CO5	2	1	3	1	-	1	3	3	-

P20CCP101	TECHNICAL REPORT WRITING AND SEMINAR	L	T	P	C	Hrs
		-	-	4	2	45

Course Objectives

- To develop their scientific and technical reading and writing skills that they need to understand and construct research articles
- To obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas

Course Outcomes

After completion of the course, the students will be able to

CO1 - Select a subject, narrowing the subject into a topic**. (K2)**

CO2 - Explain objective and collect the relevant bibliography**. (K2)**

CO3 - Describe the papers and understand the author's contributions and critically analyzing each paper. **(K2)**

CO4 - Prepare a working outline and linking the papers and preparing a draft of the paper. **(K2)**

CO5 - Prepare conclusions based on the reading of all the papers, Writing the Final Paper, and giving final Presentation. **(K2)**

Activity	**Instructions**	**Submission week**	**Evaluation**
Selection of area of interest and Topic	select an area of interest, topic and state an objective	2nd week	**3 %** Based on clarity of thought, current relevance and clarity in writing
Stating an Objective			
Collecting Information about area & topic	• List 1 Special Interest Groups or professional society • List 2 journals • List 2 conferences, symposia or workshops • List 1 thesis title • List 3 web presences (mailing lists, forums, news sites) • List 3 authors who publish regularly in your area • 7. Attach a call for papers (CFP) from your area.	3rd week	**3%** (the selected information must be area specific and of international and national standard)
Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter	• provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar • When picking papers to read - try to: - Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them. - Favor papers from well-known journals and conferences, in the field (as indicated in other Favor more recent papers, - Pick a recent survey of the field so you can quickly gain an overview, Find relationships with respect to each other and to your topic area (classification	4th week	**6%** (the list of standard papers and reason for selection)

	scheme/categorization) - Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered		
Reading and notes for first 5 papers	Reading Paper Process For each paper form a Table answering the following questions: • What is the main topic of the article? • What was/were the main issue(s) the author said they want to discuss? • Why did the author claim it was important? • What simplifying assumptions does the author claim to be making? • What did the author do? • How did the author claim they were going to evaluate their work and compare it to others? • What did the author say were the limitations of their research? • What did the author say were the important directions for future research? • Conclude with limitations/ issues not addressed by the paper (from the perspective of survey)	6th week	8% (The table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for next 5 papers	Repeat Reading Paper Process	7th week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper
Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th week	8% (this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th week	6% (Clarity, purpose and conclusion) 6% Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th week	5% (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11th week	10% (this component will be evaluated based on the linking and classification among the papers)
Conclusions	Write your conclusions and future work	12th week	5% (conclusions)
Final Draft	Complete the final draft of your paper	13th week	10% (formatting, English, Clarity and linking) 4% Plagiarism Check Report

Seminar	A brief 15 slides on your paper	14th & 15th week	10% (based on presentation and Viva voice)

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	3	2	1	-	1	3	-	-
CO2	2	3	2	1	-	1	3	-	-
CO3	2	3	2	1	-	1	3	-	-
CO4	2	3	2	1	-	1	3	-	-
CO5	2	3	2	1	-	1	3	-	-

SEMESTER II

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P20VET204	Advanced Digital System Design	PC	3	0	0	3	40	60	100
2	P20VET205	Embedded Networking	PC	3	0	0	3	40	60	100
3	P20VET206	Embedded System Design	PC	3	0	0	3	40	60	100
4	P20VET207	Low Power Digital VLSI Design	PC	3	0	0	3	40	60	100
5	P20VEE2XX	Professional Elective-II	PE	3	0	0	3	40	60	100
6	P20VEE2XX	Professional Elective-III	PE	3	0	0	3	40	60	100
Practical										
7	P20VEP202	Embedded System Design Laboratory	PC	0	0	4	2	50	50	100
8	P20CCP202	Seminar on ICT a hands-on approach	PC	0	0	4	2	100	-	100
Audit Course										
9	P20ADC20X	Audit Course-II	AC	-	-	2	-	100	-	100
Employability Enhancement Course										
10	P20VEC2XX	Employability Enhancement Course-II	EEC	-	-	4	-	100	-	100
Total							**22**	**590**	**410**	**1000**

P20VET204	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C	Hours
		3	-	-	3	45

Course Objectives

- To learn about sequential machines and ASM charts
- To design asynchronous and to learn about hazards and race occurrences in it
- To learn and design Finite State Machines
- To identify faults in circuits using various design methods
- To simulate the designed digital circuits

Course Outcomes

After completion of the course, students will be able to

CO1 - Realize the Algorithmic State Machine. **(K3)**
CO2 - Design and analyze the asynchronous sequential digital circuits. **(K3)**
CO3 - Design and analyze the synchronous sequential circuits using PLDs. **(K3)**
CO4 - Identify the fault in the digital circuits. **(K3)**
CO5 - Simulate and synthesis the sequential circuits. **(K4)**

UNIT I SEQUENTIAL CIRCUIT DESIGN (9 Hrs)

Analysis of clocked synchronous sequential circuits and modeling- state diagram - state table - state table assignment and reduction - design of iterative circuits - ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN (9 Hrs)

Analysis of asynchronous sequential circuit: Design of asynchronous sequential circuit - static and dynamic methods - flow table reduction - races - state assignment transition table and problems in transition table - essential hazards - data synchronizers - mixed operating mode asynchronous circuits

UNIT III SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES (9 Hrs)

Programming logic device families: Designing a synchronous sequential circuit using PLA/PAL - realization of finite state machine using PLD/FPGA.

UNIT IV FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS (9 Hrs)

Fault diagnosis method: Path sensitization method - Boolean difference method - D – algorithm - tolerance techniques - compact algorithm - fault in PLA/PAL- test generation - DFT schemes - built in self-test

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Simulation of synchronous/ asynchronous sequential circuits: Logic compilation - two level and multi-level logic synthesis - sequential logic synthesis -technology mapping - tools for mapping to PLDs and FPGAs

Text Books

1. Charles H R Jr, Larry L K, “Fundamentals of Logic Design “, 7th Edition, Global Engineering, 2014.
2. Parag K L, ‘Fault Tolerant and Fault Testable Hardware Design” 1st Edition, B S Publications, 2002.
3. ParagK.L, “Digital system Design using PLD “, B S Publications,2003

Reference Books

1. Nripendra N B,, Logic Design Theory Prentice Hall of India, 1993.
2. Charles H RJr, Digital System Design using VHDL ǁ, 2nd Edition, CL Engineering, 2007
3. Michael D C, “Modeling, Synthesis, and Rapid Prototyping with the VERILOG HDL”, Prentice Hall, 2006.
4. O. Hamblen, T. S. Hall, and M. D. Furman, "Rapid Prototyping of Digital Systems", SPOC Edition, Springer, 2008
5. Stephen Brown, and Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design", Third Edition, McGraw-Hill, 2014.

Web References

1. http://nptel.ac.in/courses/117108040/downloads/Digital%20System%20Design.pdf
2. https://www.doulos.com/knowhow/verilog_designers_guide/
3. https://www.nandland.com/
4. https://lecturenotes.in/notes/15423-note-for-digital-system-design-dsd-by-vtu-rangers
5. https://www.sjsu.edu/people/thuy.le/docs/271syl.pdf

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	3	-
CO2	2	-	3	3	-	1	3	3	-
CO3	2	-	3	3	-	1	3	3	-
CO4	2	-	3	3	-	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VET205 EMBEDDED NETWORKING

L	T	P	C	Hours
3	-	-	3	45

Course Objectives

- To learn about serial and parallel communication protocols
- To learn about USB and CAN buses used in embedded system
- To learn about Ethernet cables used for LAN communication
- To learn about various web service protocols
- To understand the working of serial and parallel communication protocols used in industry

Course Outcome

After completion of the course, the students are able to

CO1 - Illustrate the type of communication protocol needed based on application. **(K3)**
CO2 - Interface the microcontroller using USB and CAN buses. **(K3)**
CO3 - Explain the working of Ethernet cables. **(K2)**
CO4 - Describe the web services various protocols. **(K3)**
CO5 - Analyze the communication protocols used by industries. **(K4)**

UNIT- I EMBEDDED COMMUNICATION PROTOCOLS (9 Hrs)

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols - RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming -ISA/PCI Bus protocols - Fire wire

UNIT- II USB AND CAN BUS (9 Hrs)

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets – Data flow types –Enumeration –Descriptors –PIC-18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN

UNIT- III ETHERNET BASICS (9 Hrs)

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol. Gigabit Ethernet

UNIT- IVEMBEDDED ETHERNET (9 Hrs)

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure

UNIT- VINSTRUCTIONAL ACTIVITY (9 Hrs)

Serial and parallel protocols used in industries – its timing diagram, Serial communication with an Arduino, visualize the Ethernet traffic using protocol analyzer

Text Books

1. Frank Vahid, Givargis, “Embedded Systems Design: A Unified Hardware/Software Introduction”, Wiley Publications, 2012.
2. Jan Axelson, “Parallel Port Complete”, Penram publications,2005.
3. Dogan Ibrahim, “Advanced PIC microcontroller projects in C”, Elsevier 2008.

Reference Books

1. Gul N. Khan, Krzysztof Iniewski,” Embedded and Networking Systems: Design”, Software, and Implementation Taylor & Francis Inc, 2013
2. Gregory J. Pottie,William J. Kaiser, “Principles of Embedded Networked Systems Design”, Cambridge University Press, 2010.
3. Jan Axelson, “Embedded Ethernet and Internet Complete”, Penram Publishing (India) Pvt. Ltd., 2003.
4. ZainalabeNavabi, “Digital System Test and Testable Design: Using HDL Models and Architectures”, Springer, 2010
5. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House

Web References

1. https://ocw.mit.edu/search/ocwsearch.htm?q=embedded%20networking
2. https://users.ece.cmu.edu/~koopman/lectures/index.html
3. http://emanager.srmist.edu.in/elibrary/temp/CAN_and_CANopen.pdf
4. https://www.iare.ac.in/sites/default/files/lecture_notes/ESD%20NOTES-A70440.
5. https://nptel.ac.in/courses/108/105/108105057/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	-	3
CO2	2	-	3	3	-	1	3	-	3
CO3	2	-	3	3	-	1	3	-	3
CO4	2	-	3	3	-	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

P20VET206 EMBEDDED SYSTEM DESIGN

L	T	P	C	Hours
3	-	-	3	45

Course Objectives

- To learn about various kinds of processors available in embedded system
- To learn the design flow of single purpose processor
- To learn the design flow of general-purpose processor
- To learn about the operating system needed for embedded system
- To learn about 8051 and FDCT

Course Outcome

After completion of the course, the students are able to

CO1 - Classify the type of processor needed for the application. **(K4)**
CO2 - Design and optimize the single purpose processor. **(K3)**
CO3 - Design Application Specific Instruction set Processors. **(K3)**
CO4 - Illustrate OS needed for embedded operation. **(K3)**
CO5 - Design a project based on 8051 with FDCT implementation. **(K3)**

UNIT- I INTRODUCTION (9 Hrs)

Embedded system overview, Design challenge: Optimizing design metrics, Processor Technology, General purpose Processors, Single purpose Processors, and Application Specific Processors, IC Technology: Full custom/VLSI, Semicustom ASIC, PLD, Trends, Design Technology

UNIT- II CUSTOM SINGLE PURPOSE PROCESSOR (9 Hrs)

RTL combinational components, RTL sequential components, Custom Single purpose Processor Design, RTL Custom Single purpose Processor Design, Optimizing Custom Single Purpose Processors, Optimizing the original program, Optimizing the FSMD, Optimizing the data path, optimizing the FSM

UNIT- III GENERAL PURPOSE PROCESSORS (9 Hrs)

Basic architecture, Data path, Control UNIT, Memory Instruction execution and Pipelining, Superscalar and VLIW architectures. Application Specific Instruction set Processors (ASIP's), Microcontrollers, DSP, Less General ASIP environments, Selecting a Microprocessor and General-purpose Processor Design

UNIT- IVEMBEDDED OS (9 Hrs)

Creating embedded operating system: Basis of a simple embedded OS, Introduction to sEOS, Using Timer 0 and Timer 1, Portability issue, Alternative system architecture, Important design considerations when using sEOS

UNIT- VINSTRUCTIONAL ACTIVITY (9 Hrs)

Study of Digital Camera- Example-User's perspective, Designer's perspective, Requirements, Specification, Informal functional specification, Nonfunctional specification, Executable specification. Design and Implementation of 8051 based design, Implementation of Fixed point FDCT, Implementation of Hardware FDCT

Text Books

1. Frank Vahid and Tony Givargis, "Embedded System Design A Unified Hardware/Software Introduction", John Wiley & Sons,2014.
2. Steve Heath, "Embedded System Design", Butterworth Heinemann, 2010.
3. Gajski and Vahid, "Specification and Design of Embedded systems", Prentice Hall, 2006.

Reference Books

1. Rajkamal, 'Embedded System", Tata McGraw Hill, 2003
2. Charls Roth, "Digital system Design using VHDL", TMH, 2007
3. Rettberg, A.; Zanella, M.; Domer, R.; Gerstlauer, A.; Rammig, F.Embedded System Design: Topics, Techniques and Trends, Springer , 2007.
4. C.M. Krishna, Kang G.Shin, "Real Time Systems" The McGraw Hill International Editions Computer Science Series , 2008.
5. : L. B. Das Pearson, "Embedded Systems" Pearson education, 2010.

Web References

1. https://lecturenotes.in/subject/557/embedded-system-design-esd
2. https://nptel.ac.in/courses/106/105/106105159
3. https://www.brainkart.com/subject/Embedded-Systems-Design_124
4. https://examupdates.in/embedded-systems-pdf/
5. https://users.ece.cmu.edu/~koopman/lectures/index.html

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	-	3
CO2	2	-	3	3	-	1	3	-	3
CO3	2	-	3	3	-	1	3	-	3
CO4	2	-	3	3	-	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

P20VET207 LOW POWER DIGITAL VLSI DESIGN

L	T	P	C	Hours
3	-	-	3	45

Course Objectives

- To learn about static and dynamic power dissipation
- To learn about various power analysis method using simulation
- To understand the operation of circuit by sizing and switching of transistors
- To know about various energy recovery techniques
- To learn about SRAM and DRAM power dissipation

Course Outcome

After completion of the course, the students are able to

CO1 - Illustrate the type of power dissipation occurring in VLSI circuits. **(K3)**
CO2 - Analyze the power dissipation in VLSI circuits. **(K4)**
CO3 - Design and simulate VLSI circuits by different gate sizing and signal gating parameter. **(K3)**
CO4 - Classify and design the type of energy recovery model needed for the VLSI circuit. **(K4)**
CO5 - Simulate and analyze the power dissipation in SRAM and DRAM memories. **(K4)**

UNIT- I POWER DISSIPATION (9 Hrs)

Introduction: Need for low power circuit design - sources of power consumption -design methodology - low power figure of merits - limits and applications of low power VLSI Design

UNIT- II POWER ANALYSIS (9 Hrs)

Power Analysis: SPICE circuit simulation - discrete transistor modeling and analysis - gate level 0 logic simulation - architecture level analysis - data correlation analysis; Probabilistic Power Analysis: Random logic signals - probabilistic power analysis techniques - signal entropy

UNIT- III CIRCUIT AND LOGIC LEVEL (9 Hrs)

Circuit Level: Transistor and gate sizing - equivalent pin ordering - network restructuring and reorganization - special latches and flip flops; Logic Level: Gate reorganization - signal gating - logic encoding - precomputation logic

UNIT- IVENERGY RECOVERY TECHNIQUES (9 Hrs)

Energy Recovery Techniques: Energy dissipation using the RC model - energy recovery circuit design - power reduction in clock networks - low power bus - delay balancing

UNIT- VINSTRUCTIONAL ACTIVITY (9 Hrs)

Simulation Study: Sources of power dissipation in SRAMs - Low power SRAM circuit techniques; Sources of power dissipation in DRAMs - Low power DRAM circuit techniques using related tools

Text Books

1. Kaushik R and Sharat C P, “Low-Power CMOS VLSI Circuit Design”, Wiley Student Edition, 2009.
2. Gary K Y, “Practical Low Power Digital VLSI Design “, Kluwer Academic Publishers, 1998.
3. Bellaouar A and Elmasry M, “Low-Power Digital VLSI Design: Circuits and Systems”, Kluwer Academic Publishers, 1995

Reference Books

1. Kiat-Seng Y and Kaushik R, “Low-Voltage, Low-Power VLSI Subsystems”, TMH Professional Engineering, 2009
2. Soudris D, Piguet C and Goutis C, “Designing CMOS Circuits for Low Power”, Kluwer Academic Publishers, 2002
3. Chandrakasan A and Robert W B, “Low-Power CMOS Design”, Wiley-IEEE Press, 2006.
4. Rabaey J M and Massoud P, “Low Power Design Methodologies”, Kluwer Academic Publishers, 2010.
5. Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits – Analysis and Design”, TMH, 2011.

Web References

1. http://www.eeherald.com/section/design-guide/Low-Power-VLSI-Design.html
2. https://nptel.ac.in/courses/106/105/106105034/
3. https://lecturenotes.in/m/30442-low-power-digital-vlsi-design
4. https://link.springer.com/content/pdf/bfm%3A978-81-322-1937-8%2F1
5. https://www.egr.msu.edu/classes/ece410/salem/files/s16/lectures/Ch2_S2_N

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	3	-
CO2	2	-	3	3	-	1	3	3	-
CO3	2	-	3	3	-	1	3	3	-
CO4	2	-	3	3	-	1	3	3	-
CO5	2	2	3	3	3	1	3	3	-

		L	T	P	C	Hours
P20VEP202	**EMBEDDED SYSTEM DESIGN LABORATORY**	**-**	**-**	**4**	**2**	**45**

Course Objectives

- To learn about RS232 cable for communication
- To design simple circuits using PIC and Arduino microcontroller
- To design various real time projects using microcontroller
- To transfer data by wireless communication
- To learn about raspberry Pi processor for real time application

Course Outcome

After completion of the course, the students are able to

CO1 - Interface a microcontroller to PC for communication. **(K3)**
CO2 - Interface various sensors using PIC and Arduino microcontrollers. **(K3)**
CO3 - Design various microcontroller-based systems**. (K3)**
CO4 - Communicate wirelessly using microcontroller. **(K3)**
CO5 - Process an image using Raspberry pi. **(K5)**

Microcontroller Based Experiments

1. Interfacing the microcontroller to a PC through RS232 and displaying the messages sent by the microcontroller on the PC.
2. Design with PIC and Arduino Microcontrollers - Assembly or C Programming/Arduino IDE programming to interface
    - 7 segment displays to display the measured voltage from 0 to 5 volts
    - LDR and display light intensity in 7 segment display
    - Temperature sensor and display temperature in 7 segment display
    - Pressure sensor and display measured pressure in 7 segment display
    - PH sensor and display measured value in 7 segment display
    - Ultrasonic sensor and display distance in 7 segment display
    - Noise sensor and display noise level in 7 segment display
3. Interface DC motor with Microcontroller and control its speed and direction using PWM
4. Microcontroller based system design
    - Lamp controller using a light sensor and a timer
    - Water Pump Controller to maintain water level in a tank
    - Moisture controller using moisture and sprinkler controller
5. Design Real time clock
6. Wireless data transfer using Microcontroller
7. Color identification and tracking using Raspberry pi

Reference Books

1. Elaf A. Saeed, “Basics Labs for Embedded Systems Using Arduino: Arduino based projects”, LAP Lambert Academic Publishing, 2020
2. Tim Wilmshurst, “Designing Embedded Systems with PIC Microcontrollers: Principles and Applications”, Elsevier Science & Technology, 2011
3. Rajkamal, ‘Embedded System”, Tata McGraw Hill, 2003
4. Charls Roth, “Digital system Design using VHDL”, TMH, 2007
5. Rettberg, A.; Zanella, M.; Domer, R.; Gerstlauer, A.; Rammig, F.Embedded System Design: Topics, Techniques and Trends, Springer , 2007.

Web References

1. http://embedded-lab.com/
2. https://www.electronics-lab.com/embedded-systems-online-training-resources/
3. https://lecturenotes.in/subject/557/embedded-system-design-esd
4. https://examupdates.in/embedded-systems-pdf/
5. https://users.ece.cmu.edu/~koopman/lectures/index.html

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	1	3	3	3	1	3	-	3
CO2	2	1	3	3	3	1	3	-	3
CO3	2	1	3	3	3	1	3	-	3
CO4	2	1	3	3	3	1	3	-	3
CO5	2	1	3	3	3	1	3	-	3

P20CCP202	SEMINAR ON ICT: A HANDS-ON APPROACH	L	T	P	C	Hrs
		-	-	4	2	45

Course Objectives

- To develop their technical reading and presentation skills that they need to understand and present using ICT Tools.
- To obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and practice to present.

Course Outcomes

After completion of the course, the students will be able to

CO1 - Select a topic, narrowing the topic into presentation.
CO2 - State an objective and use the relevant ICT tools to make the presentation effective.
CO3 - Study the topic and understanding the contributions and prepare report.
CO4 - Prepare a working demo.
CO5 - Prepare conclusions based on the reading of the topic and giving final Presentation.

The methodology used is “learning by doing”, a hands-on approach, enabling the students to follow their own pace. The teacher, after explaining the project, became a tutor, answering questions and helping students on their learning experience.

CT skills

- Understand ICT workflow in cloud computing.
- Manage multitasking.
- Deal with main issues using tech in class.
- Record, edit and deliver audio and video.
- Automate assessments and results.

Teaching tools

- Different ways to create audiovisual activities.
- Handle audiovisual editors.
- Collaborative working.
- Individualize learning experience.
- Get instant feedback from students.

Each one of the students will be assigned an ICT Topic and the student has to conduct a detailed study on the assigned topic and prepare a report, running to 30 or 40 pages for which a demo to be performed followed by a brief question and answer session. The demo will be evaluated by the internal assessment committee (comprising of the Head of the Department and two faculty members) for a total of 100 marks.

P20ECC2XX EMPLOYABILITY ENHANCEMENT COURSES

L	T	P	C	Hrs
0	0	4	-	50

Students shall choose an International certification course offered by the reputed organizations like Google, Microsoft, IBM, Texas Instruments, Bentley, Autodesk, Eplan and CISCO, etc. The duration of the course is 40-50 hours specified in the curriculum, which will be offered through Centre of Excellence.

Pass /Fail will be determined based on participation, attendance, performance and completion of the course. If a candidate fails, he/she must repeat the course in the subsequent years. Pass in this course is mandatory for the award of degree.

P20VEW301	PROJECT PHASE I	L	T	P	C
		0	0	12	6

Aim & Objective:

The project work aims to develop the work practice and to apply theoretical and practical tools/techniques for solving real life problems related to industry and current research. The objective of the project work is to improve the professional competency and research attitude by touching the areas which are not covered in theory or laboratory classes.

- The project work shall be a design project/experimental project and/or computer simulation project on any of the topic in manufacturing engineering or related field.
- The project work shall be allotted individually on different topics.
- The students shall be encouraged to do their project work in the parent institute itself. In exceptional cases the students shall be permitted to undertake continue their project outside the parent institute with appropriate permission from Head of the institution through the Project Coordinator.
- Department shall constitute an Evaluation Committee to review the project work.
- The Evaluation committee shall consist of at least three faculty members namely internal guide, project coordinator and another expert in the specified area of the project.

The student is required to undertake the project phase I during the third semester and the same shall be continued in the 4thsemester (Phase II). Phase I consist of preliminary thesis work, three reviews of the work and the submission of preliminary report. First review shall highlight the topic, objectives and origin of problem, second review shall highlight, Literature survey, methodology and expected results. Third review shall evaluate the progress of the work, preliminary report and scope of the work which shall be completed in the 4thsemester. Also, the evaluation of project phase - I shall be done externally.

P20VEW302	INTERNSHIP	L	T	P	C
		0	0	0	2

Students should undergo training or internship during summer / winter vacation at Industry/ Research organization / University (after due approval from the Programme Academic Coordinator and Department Consultative Committee (DCC). In such cases, the internship/training should be undergone continuously (without break) in one organization. Normally no extension of time is allowed. However, DCC may provide relaxation based on the exceptional case. The students can undergo three to four weeks of internship in established industry / Esteemed institution during vacation period. The student should give presentation and send report to DCC. The Internship is assessed internally for 100 marks.

P20VES301	NPTEL/GIAN/MOOC	L	T	P	C
		0	0	0	-

Student should register online courses like MOOC / SWAYAM / NPTEL etc. approved by the Department committee comprising of HoD, Programme Academic Coordinator and Subject Experts. Students have to complete relevant online courses successfully. The list of online courses is to be approved by Academic Council on the recommendation of HoD at the beginning of the semester if necessary, subject to ratification in the next Academic council meeting. The Committee will check the progress of the student and recommend the grade (100% Continuous Assessment pattern) based on the marks secured in online examinations. The marks attained for this course is not considered for CGPA calculation.

P20VEW403	` PROJECT PHASE II	L	T	P	C
		0	0	24	12

Aim & Objective:

The project work aims to develop the work practice and to apply theoretical and practical tools/techniques for solving real life problems related to industry and current research. The objective of the project work is to improve the professional competency and research attitude by touching the areas which are not covered in theory or laboratory classes.

- The project work shall be a design project/experimental project and/or computer simulation project on any of the topic in manufacturing engineering or related field.
- The project work shall be allotted individually on different topics.
- The students shall be encouraged to do their project work in the parent institute itself. In exceptional cases the students shall be permitted to undertake continue their project outside the parent institute with appropriate permission from Head of the institution through the Project Coordinator.
- Department shall constitute an Evaluation Committee to review the project work.
- The Evaluation committee shall consist of at least three faculty members namely internal guide, project coordinator and another expert in the specified area of the project.

Project phase II is a continuation of project phase I which started in the third semester. There shall be three reviews in the fourth semester, first in the beginning of the semester, second in the middle of the semester and the Third at the end of the semester. First review is to evaluate the progress of the work and planned activity; second review shall be presentation and discussion. Third review shall be a pre-submission presentation before the evaluation committee to assess the quality and quantity of the work done. This would be a prequalifying exercise for the students for getting approval for the submission of the thesis. At least one technical paper shall be prepared for possible publication in journals or conferences. The technical paper shall be submitted along with the thesis. The final evaluation of the project shall be done externally.

PROFESSIONAL ELECTIVE – I

Sl. No.	Course Code	Course Title	Periods			Credits	Max. Marks		
			L	T	P		CAM	ESM	Total
1	P20VEE101	Embedded Technology	3	-	-	3	40	60	100
2	P20VEE102	Advanced Microprocessor and Interfacing	3	-	-	3	40	60	100
3	P20VEE103	Modeling and Synthesis with Verilog HDL	3	-	-	3	40	60	100
4	P20VEE104	Physical Design of VLSI	3	-	-	3	40	60	100
5	P20VEE105	Software for Embedded System	3	-	-	3	40	60	100

P20VEE101	EMBEDDED TECHNOLOGY	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To states the basics of OSI reference model and RTOS
- To explain the modules and tasks of software partitioning
- To discuss about the various techniques of Tables and data structures
- To analyze the performance of hardware using management software
- To demonstrate the embedded system model with instruction

Course Outcomes

After completion of the course, the students will be able to

CO1 - Explain the basics of OSI reference model and RTOS. **(K2)**
CO2 - Comprehends the modules and tasks of software partitioning. **(K3)**
CO3 - Applies the various techniques of Tables and data structures. **(K3)**
CO4 - Manipulates the performance of hardware using management software. **(K3)**
CO5 - Evaluates the model of embedded system with instruction. **(K3)**

UNIT I OSI REFERENCE MODEL (9 Hrs)

Communication Devices – Communication Echo System – Design Consideration – Host Based Communication – Embedded Communication System – OS Vs RTOS.

UNIT II SOFTWARE PARTITIONING (9 Hrs)

Limitation of strict Layering – Tasks & Modules – Modules and Task Decomposition – Layer2 Switch – Layer3 Switch / Routers – Protocol Implementation – Management Types – Debugging Protocols.

UNIT III TABLES & OTHER DATA STRUCTURES (9 Hrs)

Partitioning of Structures and Tables – Implementation – Speeding Up access – Table Resizing – Table access routines – Buffer and Timer Management – Third Party Protocol Libraries.

UNIT IV MANAGEMENT SOFTWARE (9 Hrs)

Device Management – Management Schemes – Router Management – Management of Sub System Architecture – Device to manage configuration – System Start up and configuration.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Implementation of 7-layer OSI in CIM: A case study, connecting a classified network to the Internet – Embedded Communication System- An internet Routing and firewall security- Simulation of Partitioning of Structures, Simulation of Speeding Up access.

Text Books

1. Sridhar. T, Designing Embedded Communication Software, CMP Books, 2003.
2. Larry L Peterson, Computer Networks: A Systems Approach, Morgan Kaufmann, 2007.
3. Edward Insam, TCP/IP Embedded Internet Applications, Newness, 2003.

Reference Books

1. Bruce Powel Douglas, Design Patterns for Embedded Systems in C, Newness, 2011.
2. Daneil W. Lewis, Fundamentals of Embedded Software, Prentice Hall 2004.
3. Richard Fabian, Data-oriented design: software engineering for limited resources and short schedules, Richard Fabian, 2018
4. Martin Särnberger, Internet Technology: With the OSI model, Lightning Source Inc, 2020
5. Gerry Howser, Computer Networks and the Internet: A Hands-On Approach, Springer Nature Switzerland AG, 2019

Web References

1. https://www.crcpress.com/Designing-Embedded-Communications-Software
2. ieeexplore.ieee.org/abstract/document/6976507
3. http://nptel.ac.in/courses/117106030/35
4. https://link.springer.com
5. https://sans.org

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	-	3
CO2	2	-	3	3	-	1	3	-	3
CO3	2	-	3	3	-	1	3	-	3
CO4	2	-	3	3	-	1	3	-	3
CO5	2	1	3	3	3	1	3	-	3

P20VEE102	ADVANCED MICROPROCESSOR AND INTERFACING	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To introduce the concepts in internal programming model of Intel family of microprocessors
- To introduce the programming techniques using MASM, DOS and BIOS function calls
- To understand architecture of PIC microcontroller and its assembly language programming
- To study internal peripherals of PIC microcontroller
- To develop real time systems using microcontrollers

Course Outcomes

After completion of the course, the students will be able to

CO1 - Explain advanced microprocessor architecture. **(K2)**
CO2 - Interpret modular programming concepts. **(K4)**
CO3 - Describe organization PIC16F877 microcontrollers. **(K2)**
CO4 - Interface peripheral devices with PIC16F877 Microcontrollers. **(K3)**
CO5 - Design and develop on Microcontroller Based system design. **(K4)**

UNIT I ADVANCED MICROPROCESSOR ARCHITECTURE (9 Hrs)

Internal Microprocessor Architecture-Real mode memory addressing – Protected Mode Memory addressing – Memory paging - Data addressing modes – Program memory addressing modes – Stack memory addressing modes – Data movement instructions – Program control instructions- Arithmetic and Logic Instructions.

UNIT II MODULAR PROGRAMMING AND ITS CONCEPTS (9 Hrs)

Fundamental of high level synthesis, Logic synthesis, Logic optimization and technology mapping, Lookup table technology mapping, Timing analysis, Timing optimization, Area optimization

UNIT III PIC MICROCONTROLLER (9 Hrs)

Architecture – memory organization – addressing modes – instruction set – PIC programming in Assembly & C –I/O port, Data Conversion, RAM & ROM Allocation, Timer programming.

UNIT IV PERIPHERAL OF PIC MICROCONTROLLER (9 Hrs)

Timers – Interrupts, I/O ports- I2C bus-A/D converter-UART- CCP modules -ADC, DAC and Sensor Interfacing –Flash and EEPROM memories.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Microcontroller based system design: Interfacing LCD Display – Keypad Interfacing - Generation of Gate signals for converters and Inverters - Motor Control – Controlling DC/ AC appliances – Measurement of frequency – Standalone Data Acquisition System.

Text Books

1. Danny Causey, Rolin McKinlay and Muhammad Ali Mazidi 'PIC Microcontroller and Embedded Systems: Using Assembly and C for PIC18', Microdigitaled, 2016
2. Daniele Lacamera, 'Embedded Systems Architecture: Explore architectural concepts, pragmatic design patterns, and best practices to produce robust systems', Packt Publishing Limited, 2018
3. Marilyn Wolf 'PIC Embedded System Interfacing: Design for the Internet-of-Things (IoT) and Cyber-Physical Systems (CPS)', Elsevier Science & Technology, 2019

Reference Books

1. MykePredko, "Programming and customizing the 8051 microcontrollers", Tata McGraw Hill, 2001.
2. Rajkamal,". Microcontrollers-Architecture, Programming, Interfacing & System design",2nd edition, Pearson, 2012.
3. I Scott Mackenzie and Raphael C.W. Phan, "The Micro controller", Pearson, Fourth edition 2012
4. MS Mohanamba Govindappa,". PIC Microcontroller Programming with Sample Source Code", Createspace Independent Publishing Platform, 2018
5. William Jayden,". Interfacing PIC Microcontrollers to Peripherial", Createspace Independent Publishing Platform, 2017

Web References

1. http:// www.nptel.iitm.ac.in
2. http:// www.microchip.com/design-centers/microcontrollers
3. https://learn.mikroe.com/
4. https://microcontrollerslab.com/pic-microcontroller-architecture/
5. https://nptel.ac.in/courses/117/104/117104072/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	-	3
CO2	2	-	3	3	-	1	3	-	3
CO3	2	-	3	3	-	1	3	-	3
CO4	2	-	3	3	-	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

P20VEE103	MODELLING AND SYNTHESIS WITH VERILOG HDL	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To learn the basics of Verilog HDL with various levels of modeling
- To classify the various delay models with behavioral description of digital circuits
- To learn the synthesis of combinational and sequential circuits
- To learn the synthesis of digital circuits in switch level modeling
- To build the higher end circuits using CAD tools

Course Outcomes

After completion of the course, the students will be able to

CO1 - Recognize the basic conventions of Verilog HDL. **(K2)**

CO2 - Define the various delay models of behavioural level description. **(K2)**

CO3 - Synthesize the combinational and sequential circuits using Verilog HDL. **(K3)**

CO4 - Synthesize the digital circuits using Switch level modeling. **(K4)**

CO5 -Carryout the HDL for various higher end circuits using CAD tool. **(K4)**

UNIT I HARDWARE MODELLING WITH VERILOG HDL (9 Hrs)

HDLs in EDA, System C, VHDL and Verilog, System Verilog overview, Hardware Encapsulation, Hardware Modeling with Verilog HDL, Hierarchical descriptions of hardware, Structured design methodology, Arrays, Using Verilog for synthesis, Event driven simulation and test benches, Logic system, data types and operators, User-defined primitives: Combinational behaviour, Sequential behavior.

UNIT II DELAY MODELS &BEHAVIORAL DESCRIPTION (9 Hrs)

Verilog models of propagation delay, Built-in constructs, Inertial delay, Time scales and precision, Delays, Delay effects and Pulse rejection, Race condition in Verilog, Types of race condition, Task and function, Events, Process control, Disable a block, Watchdog, debugging, Code coverage, Testing strategies, File handling, Behavioral descriptions in Verilog HDL.

UNIT III SYNTHESIS OF COMBINATIONAL LOGIC &SEQUENTIAL LOGIC (9 Hrs)

Synthesis of Combinational Logic, HDL-Based Synthesis, Technology-Independent Design, Synthesis Methodology, Styles for Synthesis of Combinational Logic, Technology Mapping and Shared Resources, Three-State Buffers, Outputs and Don't Cares, Synthesis of Sequential Logic,Latches, Edge-Triggered Flip-Flops, Registered Combinational Logic, Shift Registers and Counters

UNIT IV SYNTHESIS OF LANGUAGE CONSTRUCTS & SWITCH LEVEL MODEL (9 Hrs)

Synthesis of Language constructs, MOS Transistor Technology, Switch-Level Models, PULL gates, CMOS Transmission gates, Bi-Directional gates (Switches), Signal Strengths, Strength Reduction by Primitives, Combination and Resolution of Signal Strengths, Signal Strengths and Wired Logic

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Case Studies on VLSI Design Automation tools-An overview of the features of practical CAD tools – Modelsim - Leonardo spectrum -Xilinx ISE - Quartus II - VLSI backend tools –IC Station, Cadence and Synopsis.

Text Books

1. M,D,Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, Prentice Hall, 2006
2. Steven M. Rubin, “Computer Aids for VLSI Design”, http://www.rulabinsky.com/cavd (free online book), 1997.
3. M,G, Arnold, “Verilog Digital – Computer Design”, Prentice Hall, 2006

Reference Books

1. S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson, 2003
2. M.J.S.Smith, Application Specific Integrated Circuits, Pearson Education, 2008.
3. M.H.Rashid, Spice for Circuits and Electronics using Pspice, PHI 1995.
4. S-Edit v13.0 user guide by Tanner EDA tool.
5. Simon Monk, ‘Programming FPGAs: Getting Started with Verilog’, McGraw-Hill Education, 2016

Web References

1. http://web.ewu.edu
2. http://nptel.iitm.ac.in
3. http://www.asic-world.com/verilog/veritut.html
4. https://www.intel.com/content/www/us/en/programmable/support/training/course/ohdl1120.html
5. https://nptel.ac.in/courses/106/105/106105165/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	3	-
CO2	2	-	3	3	-	1	3	3	-
CO3	2	-	3	3	-	1	3	3	-
CO4	2	-	3	3	-	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VEE104	PHYSICAL DESIGN OF VLSI	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To acquire knowledge on fundamentals of VLSI technology
- To introduce the concept of Placement using various algorithms
- To outline the Routing methodologies using various algorithms
- To understand about various performance issues of physical design
- To apply the various physical design concepts for effective performance of circuits

Course Outcomes

After completion of the course, the students will be able to

CO1 - Explain the concepts of VLSI technology in physical design. **(K2)**
CO2 - Illustrate the concept of Placement using various algorithms. **(K3)**
CO3 - Illustrate the Routing methodologies using various algorithms. **(K3)**
CO4 -Conclude the concepts of delay modeling& delay minimization **(K3)**
CO5 -Examine single layer and over the cell routing and apply 1D and 2D compaction techniques. **(K4)**

UNIT I INTRODUCTION TO VLSI TECHNOLOGY (9 Hrs)

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein-Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array (FPGA)-layout methodologies-Packaging-Computational Complexity-Algorithmic Paradigms.

UNIT II PLACEMENT USING TOP-DOWN APPROACH (9 Hrs)

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic- Ratio-cut- partition with capacity and i/o constraints; Floor planning: Rectangular dual floor planning- hierarchical approach- simulated annealing- Floor plan sizing; Placement: Cost function- force directed method- placement by simulated annealing- partitioning placement- module placement on a resistive network – regular placement- linear placement

UNIT III ROUTING USING TOP DOWN APPROACH (9 Hrs)

Fundamentals: Maze running- line searching- Steiner trees; Global Routing: Sequential Approaches-hierarchical approaches- multi-commodity flow based techniques- Randomised Routing- One Step approach-Integer Linear Programming; Detailed Routing: Channel Routing- Switch box routing; Routing in FPGA: Array based FPGA- Row based FPGAs

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT (9 Hrs)

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Driving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization- unconstrained via Minimization- Other issues in minimization

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Planar subset problem (PSP) - Single layer global routing- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over the Cell (OTC) Routing- Multiple chip modules (MCM) - Programmable Logic Arrays- Transistor chaining- Wein-Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction

Text Books

1. Sung Kyu Lim, “Practical Problems in VLSI Physical Design Automation”, Springer-Verlag New York Inc., 2008
2. Ban Wong, Anurag Mittal Yu Cao and Greg Starr, “Nano CMOS Circuit and Physical Design” Wiley, 2004
3. N.A. Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer Academic, 2002

Reference Books

1. Sadiq M. Sait, Habib Youssef, “VLSI Physical Design Automation, Theory and Practice” World Scientific Publishing Company, 2003
2. Naveed A. Sherwani, “Algorithms for VLSI Physical Design Automation”, Springer-Verlag New York Inc., 2013
3. Erik Brunvand, “Digital VLSI Chip Design with Cadence and Synopsys CAD Tools”, Pearson, 2010
4. Andrew B Kahng, Jens Lienig and Igor L Markov, “VLSI Physical Design: From Graph Partitioning to Timing Closure”, Springer, 2011
5. Krishna Lal Baishnab and Kiran Maiye, “Convex Optimisation on Routing in VLSI Physical Design”, LAP Lambert Academic Publishing, 2017

Web References

1. http://www2.inf.uos.de/papers_html/
2. http://ic.sjtu.edu
3. http://nptel.iitm.ac.in
4. https://www.ifte.de/books/eda/chap1.pdf
5. https://nptel.ac.in/courses/106/105/106105161/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	3	-
CO2	2	-	3	3	-	1	3	3	-
CO3	2	-	3	3	-	1	3	3	-
CO4	2	-	3	3	-	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VEE105	SOFTWARE FOR EMBEDDED SYSTEMS	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To describe the basics of programming embedded systems and memory testing
- To discuss the various identifiers of python programming
- To examine the design and validation of embedded software development process
- To outline and explain the unified modeling language
- To demonstrate and exhibit various practical embedded systems

Course Outcomes

After completion of the course, the students will be able to

CO1 - List the basics of programming embedded systems and memory testing. **(K3)**
CO2 - Explain the various identifiers of python programming. **(K2)**
CO3 - Illustrate the design and validation of embedded software development process. **(K3)**
CO4 - Categorize the unified modeling language. **(K3)**
CO5 - Justify and evaluate various practical embedded systems. **(K4)**

UNIT I PROGRAMMING EMBEDDED SYSTEMS (9 Hrs)

Embedded Program – Role of Infinite loop – Compiling, Linking and locating – downloading and debugging – Emulators and simulators processor – External peripherals – Toper of memory – Memory testing – Flash Memory.

UNIT II ADDRESSING, VARIABLE AND FUNCTIONS (9 Hrs)

Overview of Embedded C - Compilers and Optimization - Programming and Assembly – Register usage conventions – typical use of addressing options – instruction sequencing – procedure call and return – parameter passing – retrieving parameters – everything in pass by value – temporary variables.

UNIT III EMBEDDED PROGRAM AND SOFTWARE DEVELOPMENT PROCESS (9 Hrs)

Program Elements – Queues – Stack- List and ordered lists-Embedded programming in C++ - Inline Functions and Inline Assembly - Portability Issues - Embedded Java- Software Development process: Analysis – Design- Implementation – Testing – Validation- Debugging - Software maintenance.

UNIT IV UNIFIED MODELING LANGUAGE (9 Hrs)

Object State Behaviour – UML State charts – Role of Scenarios in the Definition of Behavior – Timing Diagrams – Sequence Diagrams – Event Hierarchies – Types and Strategies of Operations – Architectural Design in UML Concurrency Design – Representing Tasks – System Task Diagram – Concurrent State Diagrams – Threads. Mechanistic Design – Simple Patterns.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Implement a state machine in embedded C to control RGB LED- Implement CAN bus Protocol- Testing sensors: Soil Mositure sensor-Web security - Case study: Web-based Home Automation system.

Text Books

1. David E.Simon, An Embedded Software Primer, Pearson Education, 2003.
2. Michael Barr, Programming Embedded Systems in C and C++, Oreilly, 2003.
3. H.M. Deitel, P.J.Deitel, A.B. Golldberg, Internet and World Wide Web – How to Program,3rd Edition , Pearson Education , 2001.

Reference Books

1. Daniel W.lewis, Fundamentals of Embedded Software where C and Assembly meet, PHI 2002.
2. Raj Kamal, Embedded Systems- Architecture, Programming and Design, Tata McGraw Hill, 2006.
3. Jean J. Labrosse; Jack Ganssle; Robert Oshana; Colin Walls; Keith E. Curtis; Jason Andrews; David J. Katz; Rick Gentile; Kamal Hyder; Bob Perrin, Embedded software, Newness, 2007.

4. Robert Oshana, 'Software Engineering for Embedded Systems: Methods, Practical Techniques, and Applications', Elsevier Science & Technology 2013
5. C. Ram Kumar, 'Software for Embedded Systems (SWES)' LAP Lambert Academic Publishing, 2019

Web References

1. https://www.zapmeta.ws
2. http://nptel.ac.in/courses/117106030/35
3. https://www.tutorialspoint.com/python/index.htm
4. https://www.javatpoint.com/python-tutorial
5. https://www.javatpoint.com/python-tutorial

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	-	3
CO2	2	-	3	3	-	1	3	-	3
CO3	2	-	3	3	-	1	3	-	3
CO4	2	-	3	3	-	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

PROFESSIONAL ELECTIVE – II

Sl. No.	Course Code	Course Title	Periods			Credits	Max. Marks		
			L	T	P		CAM	ESM	Total
1	P20VEE206	VLSI Architecture	3	-	-	3	40	60	100
2	P20VEE207	CAD for VLSI Circuits	3	-	-	3	40	60	100
3	P20VEE208	Design of Analog and Mixed VLSI Circuits	3	-	-	3	40	60	100
4	P20VEE209	Distributed Embedded Computing	3	-	-	3	40	60	100
5	P20VEE210	Internet of Things	3	-	-	3	40	60	100

P20VEE206	VLSI ARCHITECTURE	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To describe the various static and dynamic circuit design concepts
- To explain the different programmable logic devices with programming technology
- To understand the algorithms for various compaction terminologies
- To construct the digital circuits with analog VLSI design
- To synthesize the various digital circuits using HDL

Course Outcomes

After completion of the course, the students will be able to

CO1- Recognizes the various static and dynamic circuit design concepts. **(K3)**
CO2- Outline the different programmable logic devices with its application. **(K3)**
CO3- Solve the algorithms for various compaction terminologies. **(K3)**
CO4- Build the digital circuits with analog VLSI design. **(K3)**
CO5 - Design the various digital circuits using HDL. **(K4)**

UNIT I CMOS DESIGN (9 Hrs)

Overview of digital VLSI design Methodologies- Logic design with CMOS-transmission gate circuits-Clocked CMOS-dynamic CMOS circuits, Bi-CMOS circuits- Layout diagram, Stick diagram-IC fabrications – Trends in IC technology.

UNIT II PROGRAMMABLE LOGIC DEVICES (9 Hrs)

Programming Techniques-Anti fuse-SRAM-EPROM and EEPROM technology – Re Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects, XilinxXC9500,Cool Runner - XC-4000,XC5200, SPARTAN, Virtex - Altera MAX 7000-Flex 10KStratix.

UNIT III BASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING (9 Hrs)

System partition – FPGA partitioning – Partitioning methods- floor planning – placement physical design flow – global routing – detailed routing – special routing- circuit extraction – DRC.

UNIT IV ANALOG VLSI DESIGN (9 Hrs)

Introduction to analog VLSI- Design of CMOS 2stage-3 stage Op-Amp –High Speed and High frequency op-amps-Super MOS-Analog primitive cells-realization of neural networks.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Synthesis of the Ripple Carry Adder, Multiplier, Comparator, Shift registers and ALU circuits in CPLD devices and analyze the design with architecture.

Text Books

1. Wayne Wolf, “Modern VLSI design “Prentice Hall India,2006.
2. Samir Palnitkar, “Verilog HDL, A Design guide to Digital and Synthesis” 2nd Edition, Pearson,2005.
3. John P. Uyemera “Chip design for submicron VLSI cmos layout and simulation “, Cengage Learning India Edition”, 2011.

Reference Books

1. Kamran Eshraghian,DouglasA.pucknell and SholehEshraghian,”Essentials of VLSI circuits and system”, Prentice Hall India,2005.
2. Saradindu Panda, “Analog and Digital VLSI Circuit Design “Laxmi Publications,2015
3. Vikram Arkalgud Chandrasetty, “VLSI Design: A Practical Guide for FPGA and ASIC Implementations“,Springer-Verlag New York Inc.,2011
4. Ajit Pal, “Low-Power VLSI Circuits and Systems “, Springer, India, Private Ltd, 2016

5. Natarajan Saravana Kumar, Krishnasamy Natarajan Vijeyakumar and Karuppanan Sakthisudhan, “VLSI Architectures “, LAP Lambert Academic Publishing, 2016

Web References

1. http://courses.engr.wisc.edu/ece/ece755.html
2. http://www.ul.ie/graduateschool/course/vlsi-systems-meng.html
3. https://www.tutorialspoint.com/digital_circuits
4. https://lecturenotes.in/subject/136/analog-vlsi-design-avlsi
5. http://www.vlsisystemdesign.com.html

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	3	-
CO2	2	-	3	3	-	1	3	3	-
CO3	2	-	3	3	-	1	3	3	-
CO4	2	-	3	3	-	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VEE207	CAD FOR VLSI CIRCUITS`	L	T	P	C	Hrs
		3	-	-	3	45

Course Objective

- To understand the concept of VLSI design automation tools problem solving
- To acquire the knowledge about layout, placement and partitioning
- To study about various routing algorithm for communication.
- To identify various modelling and simulation for all the level
- To get knowledge about the interface for communication with their Applications development

Course Outcome

After completion of the course, the students will be able to

CO1- Distinguish the concept of VLSI design automation tools problem solving **(K3)**

CO2- Demonstrate the knowledge about layout, placement and partitioning **(K3)**

CO3- Contrast the various routing algorithm for communication **(K3)**

CO4- Discover the concept of various modelling and simulation for all the level **(K3)**

CO5- Operation of interface for communication with their Applications development **(K4)**

UNIT I INTRODUCTION TO VLSI DESIGN FLOW (9 Hrs)

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

UNIT II LAYOUT, PLACEMENT AND PARTITIONING (9 Hrs)

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning

UNIT III FLOOR PLANNING AND ROUTING (9 Hrs)

Floor planning concepts, Shape functions and floor plan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

UNIT IV SIMULATION AND LOGIC SYNTHESIS (9 Hrs)

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Study of Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations

Text Books

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
2. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
3. Rolf Drechsler, " Evolutionary Algorithms for VLSI CAD", Springer-Verlag New York Inc., 2010

Reference Books

1. Erik Brunvand, “Digital VLSI Chip Design with Cadence and Synopsys CAD Tools”, Pearson, 2010
2. Naveedshervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, 2005, Springer International Edition.
3. Shin-ichi Minato, "Binary Decision Diagrams and Applications for VLSI CAD", Springer-Verlag New York Inc.,2011
4. Wolfgang Fichtner, " VLSI CAD Tools and Applications", Springer-Verlag New York Inc., 2011
5. Erik Brunvand," Digital VLSI Chip Design with Cadence and Synopsys CAD Tools", Pearson Education, 2020

Web References

1. www.facweb.iitkgp.ernet.in/~isg/CAD/index.html
2. nptel.ac.in/courses/106106088/
3. https://nptel.ac.in/courses/106/106/106106089/
4. https://www.rulabinsky.com/cavd/
5. http://www.eng.auburn.edu/~nelson/courses/elec5250_6250/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	3	-
CO2	2	-	3	3	-	1	3	3	-
CO3	2	-	3	3	-	1	3	3	-
CO4	2	-	3	3	-	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VEE208	DESIGN OF ANALOG AND MIXED VLSI CIRCUITS	L	T	P	C	Hrs
		3	-	-	3	45

Course Objective

- To study analog integrated circuits of ADC and DAC Specifications
- To explain the concept of Architecture of data converter
- Understand the knowledge about SNR in data Converter and filters
- To acquire the operational amplifiers and mixed signal circuits
- To evaluate the features of Phase locked loop mixed mode VLSI circuits and differential amplifier

Course Outcome

After completion of the course, the students will be able to

CO1- Distinguish the concept of analog integrated circuits of ADC and DAC Specifications. **(K3)**

CO2- Demonstrate the concept of Architecture of data converter. **(K3)**

CO3- Contrast the about SNR in data Converter and filters. **(K3)**

CO4- Discover the concept of operational amplifiers and mixed signal circuits. **(K3)**

CO5-Operation and features of Phase locked loop mixed mode VLSI circuits and differential amplifier. **(K4)**

UNIT I DATA CONVERTERS (9 Hrs)

Data Converter Fundamentals: Analog versus digital discrete time signals - converting analog signals to data signals- sample and hold characteristics - DAC specifications - ADC specifications - mixed-signal layout issues.

UNIT II DATA CONVERTER ARCHITECTURES (9 Hrs)

Data Converter Architectures: DAC architectures - digital input code - resistors string - R-2R ladder networks - current steering - charge scaling – DACs - cyclic DAC - pipeline DAC - ADC architectures – flash ADC - 2-step flash ADC - pipeline ADC - integrating ADC - successive approximation ADC

UNIT III SNR IN DATA CONVERTERS (9 Hrs)

Data Converter SNR: Improving SNR using averaging (Excluding Jitter & averaging onwards) - decimating filters for ADCs (Excluding Decimating without averaging onwards) - interpolating filters for DAC - band pass and high pass sync. Filters.

UNIT IV OPERATIONAL AMPLIFIERS AND MIXED SIGNAL CIRCUITS (9 Hrs)

Differential amplifier- basic differential pair - Gilbert Cell; Op-Amp: Performance parameters - one stage and two stage Op-Amp - design of two stage Op-Amps - gain boosting - common mode Feedback – slew rate – offset effects –PSRR- noise – stability and frequency compensation - two stage open loop comparators–high speed comparators - sample and hold circuit- switched capacitor circuits - oscillators - VCO - PLL.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Design and simulation of different VLSI Circuits: Current mirrors - Differential Amplifier - PLL - ADC/DAC

Text Books

1. Razavi B, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill Edition, 2008.
2. Baker R J, “CMOS: Circuit Design, Layout and Simulation”, 3rd Edition, John Wiley and Sons, NJ, 2010
3. Karl Stephan, “Analog and Mixed-Signal Electronics”, John Wiley and Sons, 2015

Reference Books

1. Allen P E and Holberg D R, “CMOS Analog Circuit Design”, 3rd Edition, Oxford University Press, USA, 2012.
2. Baker R J, “CMOS: Mixed-Signal Circuit Design”, John Wiley India Edition, 2009.
3. Arjuna Marzuki, “CMOS Analog and Mixed-Signal Circuit Design: Practices and Innovations”, Taylor & Francis Ltd, 2020
4. Mourad Fakhfakh , Esteban Tlelo-cuautle and Rafael Castro-Lopez, “Analog/RF and Mixed-Signal Circuit Systematic Design”, Springer-Verlag Berlin and Heidelberg GmbH & Co. KG, 2015
5. A. Vachoux , Jean-Michel Berge , Oz Levia and Jacques Rouillard, “Analog and Mixed-Signal Hardware Description Language”, Springer-Verlag New York Inc., 2012

Web References

1. http://nptel.ac.in/courses/117101105/
2. http://nptel.ac.in/courses/117101106/
3. http://nptel.ac.in/courses/117106034/
4. https://freevideolectures.com/course/3676/cmos-mixed-signal-vlsi-design
5. https://isn.ucsd.edu/courses/492/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	3	-
CO2	2	-	3	3	-	1	3	3	-
CO3	2	-	3	3	-	1	3	3	-
CO4	2	-	3	3	-	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VEE209	DISTRIBUTED EMBEDDED COMPUTING	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To study the basic concepts of internet infrastructure and network security
- To acquire knowledge about server applications and design a HTML & XML Web page
- To design an embedded system by using java and j2ME in web technology
- To study about embedded agents for various criteria with benchmark embedded
- To provide knowledge in distributed embedded computing architecture

Course Outcomes

After completion of the course, the students will be able to

CO1- Distinguish the concept of internet infrastructure and network security. **(K3)**

CO2- Demonstrate the concept of server applications and design a HTML & XML Web page. **(K3)**

CO3- Contrast embedded systems by using java and j2ME in web technology. **(K3)**

CO4- Discover the embedded agents for various criteria with benchmark embedded. **(K3)**

CO5- Gain knowledge in distributed embedded computing architecture. **(K4)**

UNIT I INTERNET INFRASTRUCTURE (9 Hrs)

Broad Band Transmission facilities –Open Interconnection standards –Local Area Networks – Wide Area Networks –Network management – Network Security – Cluster computers.

UNIT II INTERNET CONCEPTS (9 Hrs)

Capabilities and limitations of the internet -– Interfacing Internet server applications to corporate databases HTML and XML Web page design through programming and the use of active components.

UNIT III EMBEDDED JAVA (9 Hrs)

Introduction to Embedded Java and J2ME - embedded java concepts -IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases –– Smart Card basics – Java card technology overview – Java card objects – Java card applets – Web Technology for Embedded Systems.

UNIT IV EMBEDDED AGENT (9 Hrs)

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

UNIT V INSTRUCTIONAL ACTIVITIES: EMBEDDED COMPUTING ARCHITECTURE (9 Hrs)

The product concepts- Automotive –Engine Control, Modelling the design of the Product Concept-Embedded System design and development life cycle model, Creating a basic VHDL for the entity of the memory block, Arithmetic and logic Unit.

Text Books

1. Bernd Kleinjohann, “Architecture and Design of Distributed Embedded Systems”, Springer, 2014
2. Bernd Kleinjohann, K H (Kane) Kim and Lisa Kleinjohann, “Design and Analysis of Distributed Embedded Systems”, Springer, 2014
3. M.Teresa Higuera-Toledano and Andy J. Wellings, “Distributed, Embedded and Real-time Java Systems”, Springer-Verlag New York Inc., 2012

Reference Books

1. Frank Vahid, “Embedded System Design: WITH VHDL Digital Design: A Unified Hardware/software Introduction”, John Wiley and Sons Ltd, 2007.
2. Wigglesworth,”Java Programming Advanced Topics,Cengage,2010
3. Mclaughlin,” Java & XML, O’reilly,2006.
4. Jack Ganssle “Embedded Systems”, Elsevier Publication, 2008
5. Tammy Noergaard“Embedded Systems Architecture” Elsevier Publications, 2005.

Web References

1. http://www.oracle.com/technetwork/articles/javase/rmi-corba-136641.html
2. http://www.es.ele.tue.nl/~heco/courses/ECA/index.html
3. www.pa.icar.cnr.it/cossentino/AOSETF10/docs/jamont.ppt
4. http://philip.greenspun.com/panda/databases-interfacing
5. C/C++ users Journal-http://www.cuj.com/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	-	3
CO2	2	-	3	3	-	1	3	-	3
CO3	2	-	3	3	-	1	3	-	3
CO4	2	-	3	3	-	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

P20VEE210	INTERNET OF THINGS	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To understand the basic concepts of Internet of Things (IoT)
- To understand the different components of an end-to-end IoT system
- To compare, and contrast hardware subsystems for different IoT systems
- To acquire knowledge about IEEE standard and application layers of CoAP, MQTT
- To get exposure of data analytics and Machine Learning Algorithms for IoT

Course Outcomes

After completion of the course, the students will be able to

CO1- Recognize the basic concepts of Internet of Things. (IoT) **(K3)**
CO2- Distinguish the different components of an end-to-end IoT system. **(K4)**
CO3- Compare and contrast hardware subsystems for different IoT systems. **(K4)**
CO4- Demonstrates about IEEE standard and application layers of CoAP, MQTT. **(K3)**
CO5- Procedure of data analytics and Machine Learning Algorithms for IoT. **(K4)**

UNIT I INTRODUCTION TO IOT (9 Hrs)

Physical Design and Logical Design of IoT, IoT Enabling Technologies, IoT Levels and Deployment Templates.

UNIT II MODELING AN IOT SYSTEM (9 Hrs)

Overview of Unified Modeling Language (UML). IoT Models: Domain Model, Information Model, Functional Model, Communication Model, Security Model.

UNIT III HARDWARE SUBSYSTEM OF IOT (9 Hrs)

Requirements and Constraints Sensors and Actuators. IoT: Single board computers - IoT subsystem for Cortex-M.

UNIT IV NETWORKING SUBSYSTEM FOR IOT (9 Hrs)

Overview of the Physical and MAC Layer: Ethernet-ESP, WiFi, IEEE 802.15.4, ZigBee and Bluetooth. Routing protocols: RPL, Ipv4/IPv6 – 6LowPAN, 4G & 5G networking paradigms. Application Layer protocols: CoAP, MQTT.

UNIT V INSTRUCTIONAL ACTIVITY: DATA ANALYTICS FOR IOT (9 Hrs)

Need for Data Analytics. Intelligent IoT Systems – Machine Learning Algorithms for IoT – Supervised, Unsupervised and Reinforcement learning.

Text Books

1. ArsheepBahga, Vijay Madisetti, “Internet of Things: A Hands-On Approach”, 1st edition, Orient Blackswan Private Limited, 2015.
2. UmitIsikdag, “Enhanced Building Information Models: Using IoT Services and Integration Patterns”, Springer, 2015.
3. Daniel Minoli “Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications”, Wiley, 2015.

Reference Books

1. Dieter Uckelmann, Mark Harrison, Florian Michahelles, “Architecting the Internet of Things”, Springer, 2011.
2. Samuel Greengard, “The Internet of Things (Essential Knowledge)”, MIT Press, 2015.
3. Zach Shelby, Carsten Bormann, “6LoWPAN: The Wireless Embedded Internet 6LowPAN”, John Wiley, 2009.
4. Francois, “Internet of Things – Architecture: IoT-A”, Technical Report, 2013.
5. Kai Hwang and Min Chen, “Big-Data Analytics for Cloud, IoT and Cognitive Computing”, John Wiley and Sons Ltd, 2017

Web References

1. http://www.abouttheinternetofthings.com/category/iot-features/
2. https://connectedworld.com/
3. https://nptel.ac.in/courses/106/105/106105166/
4. https://lecturenotes.in/subject/370/internet-of-things-iot
5. https://www.codeproject.com/Learn/IoT/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	-	3
CO2	2	-	3	3	-	1	3	-	3
CO3	2	-	3	3	-	1	3	-	3
CO4	2	-	3	3	-	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

PROFESSIONAL ELECTIVE – III

Sl. No.	Course Code	Course Title	Periods			Credits	Max. Marks		
			L	T	P		CAM	ESM	Total
1	P20VEE211	DSP Processor Architecture and Programming	3	-	-	3	40	60	100
2	P20VEE212	Industrial Automation using PLC and SCADA	3	-	-	3	40	60	100
3	P20VEE213	Principles of ASIC Design	3	-	-	3	40	60	100
4	P20VEE214	Real Time Systems	3	-	-	3	40	60	100
5	P20VEE215	Testing of VLSI Circuits	3	-	-	3	40	60	100

P20VEE211	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To understand concept of basic level processor consideration
- To acquire the knowledge about architecture of TMS320C Series
- How to implement TMS320C Series in fast Fourier transform
- To understand the concept of implementation of IIR & FIR in Digital processor technologies
- To design and implement a variety of algorithms for real world applications

Course Outcomes

After completion of the course, the students will be able to

CO1 - Distinguish the various Data representations and Processors. **(K4)**
CO2 - Construct and analysis of various architecture of TMS320C Series. **(K4)**
CO3 - Compute and illustrate the Fast Fourier transform of TMS320C Series. **(K3)**
CO4 - Explains and compares DFT & FFT of fixed- and floating-point representation. **(K2)**
CO5 - Summarise the various algorithms for real world applications. **(K4)**

UNIT I DIGITAL SIGNAL PROCESSING SYSTEMS (9 Hrs)

Introduction to Digital signal processor architectures – Software developments – Hardware issues – System considerations – Implementation considerations, Data representations, Finite word length effects, Programming issues, Real time implementation considerations.

UNIT II DIGITAL SIGNAL PROCESSORS (9 Hrs)

TMS320C62x AND TMS320C64x - Architecture overview, Memory systems, External memory addressing, Instruction set, Programming considerations, system issues. TMS320C67X – Architecture overview, Instruction set, Pipeline Architecture, Programming considerations, Real time implementations.

UNIT III IMPLEMENTATION OF FAST FOURIER TRANSFORMS (9 Hrs)

Introduction to DFT – FFT algorithms – Decimation-in-time, Decimation-in-frequency - Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

UNIT IV FIR AND IIR FILTER IMPLEMENTATIONS (9 Hrs)

FIR and IIR filters – Characteristics, Structures, FIR Filter design using Windowing and frequency sampling method, IIR Filter-Butterworth and Chebyshev Filter Design-, Fixed point implementation using TMS320C64x, Floating point implementation using TMS320C67x.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Design a FIR, IIR filter and implement in DSP processor. Develop programs to perform various process of convolution, DFT, FFT algorithm. Digital Signal Processor based experiments: Auto Correlation and Cross correlation. Linear and circular Convolution. DFT/FFT. Design of FIR filter. Design of IIR filter

Text Books

1. John G Proakis and Manolakis, “Digital Signal Processing Principles, Algorithms and Applications”, Pearson, Fourth Edition, 2007
2. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, Cengage Learning India Private Limited, Delhi 2012.
3. Rulph Chassaing and Donald Reay, Digital Signal Processing and Applications with the C6713 and C6416 DSK, John Wiley and Sons, Inc., Publication, 2012.

Reference Books

1. B. VenkataRamani and M. Bhaskar, “Digital Signal Processors, Architecture, Programming and Applications “ , TMH, 2004.
2. Lapsley “DSP Processor Fundamentals, Architectures & Features” S.Chand & Co, 2000, Reprint.
3. SenM.Kuo, Woon-SengS.Gan, “Digital Signal Processors – Architectures, Implementations and Applications”, Pearson Education, 2005, Second Impression, 2009.
4. A.V. Oppenheim, R.W.Schafer and J.R.Buck, "Discrete Time Signal Processing", Pearson, 2004.
5. B. Venkataramani and M. Bhaskar, Digital Signal Processors – Architecture, Programming and Applications – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.

Web References

1. http://www.nptel.iitm.ac.in/courses
2. https://link.springer.com
3. http://users.ece.utexas.edu/~bevans/hp-dsp-seminar/01_Introduction
4. http://meseec.ce.rit.edu/eecc722-fall2003/722-10-8-2003
5. https://cds.cern.ch/record/1100536/files/p167

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	-	3
CO2	2	-	3	3	-	1	3	-	3
CO3	2	-	3	3	-	1	3	-	3
CO4	2	-	3	3	-	1	3	-	3
CO5	2	2	3	3	3	1	3	-	3

P20VEE212	INDUSTRIAL AUTOMATION USING PLC AND SCADA	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To study about architecture and interfacing of PLC
- To expose programming of PLC
- To acquire the knowledge about interfacing of PLC with various circuits
- To understand the concept of SCADA based system
- To practice PLC program for real time application

Course Outcomes

After completion of the course, the students will be able to

CO1 - Describe architecture and interfacing of PLC. **(K3)**

CO2 - Write PLC program for performing fundamental logic. **(K3)**

CO3 - Interface PLC with other circuits. **(K3)**

CO4 - Interface SCADA with PLC. **(K3)**

CO5 - Use PLC and SCADA for industrial automation. **(K3)**

UNIT I PLC AND I/O PROCESSING (9 Hrs)

Programmable Logic Controller basics, overview of PLC systems – Architecture of PLC, Principle of Operation, input/output Units – power supplies and isolators, current sinking and current sourcing, types of PLC memory, fundamental PLC wiring diagram, relays, switches, transducers, sensors –seal-in circuits. Input/output units Signal conditioning. Remote connections Networks Processing inputs I/O addresses

UNIT II PROGRAMMING OF PLC: FUNDAMENTALS OF LOGIC (9 Hrs)

Programming of PLC: Fundamentals of logic, PLC programming languages. Ladder diagrams, Ladder Diagram Instruction, Logic functions, Latching, Multiple outputs. Timer and counter- types along with timing diagrams, shift registers, sequencer function, latch instruction; Arithmetic and logical instruction with various examples. ON/OFF switching devices, I/O analog devices, Analog PLC operation, PID control of continuous processes, simple closed loop systems, closed loop system using Proportional, Integral & Derivative (PID), PLC interface, and Industrial process example.

UNIT III PLC INTERFACE TO VARIOUS CIRCUITS: (9 Hrs)

PLC interface to various circuits: Encoders, transducer and advanced sensors. Measurement of temperature, flow, pressure, force, displacement, speed, level. Developing a ladder logic for Sequencing of motors, Tank level control, ON-OFF temperature control, elevator, bottle filling plant, car parking etc. Motors Controls: AC Motor starter, AC motor overload protection, DC motor controller, Variable speed (Variable Frequency) AC motor Drive

UNIT IV SCADA SYSTEMS (9 Hrs)

Introduction, Communication requirements, Desirable Properties of SCADA system, features, advantages, disadvantages and applications of SCADA. SCADA Architectures (First generation - Monolithic, second generation - Distributed, Third generation – Networked Architecture), SCADA systems in operation and control of interconnected power system, Power System Automation (Automatic substation control and power distribution). Open systems interconnection (OSI) Model, Process Field bus (Profibus). Interfacing of SCADA with PLC.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Automatic Bottle Filling System- Traffic Light Control- -Program to Control Level of Parallel Tanks- Program to Operate Drilling of Parts-Industrial project document

Text Books

1. Gary Dunning, “Introduction to Programmable Logic Controllers”, Thomson, 3rd Edition, .2006
2. John R. Hackworth, Frederick D., Hackworth Jr., “Programmable Logic Controllers Programming Methods and Applications”, PHI Publishers.2003
3. John W. Webb, Ronald A. Reis, “Programmable Logic Controllers: Principles and Application”, PHI Learning, New Delhi, 5th Edition. 2003

Reference Books

1. Stuart A. Boyer: “SCADA- Supervisory Control and Data Acquisition”, Instrument Society of America Publications, USA, The Instrumentation system and Automation Society, 4th Edition, 2010.
2. Gordon Clarke, Deon Reynders” Practical Modern SCADA Protocols: DNP3, 60870.5 and Related Systems”, Newnes An imprint of Elsevier Publications, 1st Edition, 2004.
3. Batten G. L., “Programmable Controllers”, McGraw Hill Inc., Second Edition, 1994
4. Gordan Clark, Deem Reynders, “Practical Modern SCADA Protocols”, ELSEVIER., 2004
5. P. K. Srivstava, “Programmable Logic Controllers with Applications”, BPB Publications, 2015

Web References

1. www.programmingembedded system.com
2. https://en.wikibooks.org/wiki/Embedded_Control_Systems_Design
3. http://nptel.ac.in/courses/117106030/35
4. https://link.springer.com
5. https://electrical-engineering-portal.com/download-center/books-and-guides/automation-control

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	-	3
CO2	2	-	3	3	1	1	3	-	3
CO3	2	-	3	3	1	1	3	-	3
CO4	2	-	3	3	1	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

P20VEE213 PRINCIPLES OF ASIC DESIGN

L	T	P	C	Hrs
3	-	-	3	45

Course Objectives

- To gain knowledge on programmable architectures for ASICs
- To learn the fundamentals of ASIC and its design methods
- To analyse the synthesis, Simulation and testing of systems
- To understand the physical design of ASIC
- To understand the Spartan 3E, Xilinx and vertex FPGA devices

Course Outcomes

After completion of the course, the students are able to

CO1 - Demonstrate VLSI tool-flow and appreciate FPGA architecture. **(K3)**
CO2 - Describe the concepts of ASIC design methodology, data path elements, operators, I/O cells. **(K3)**
CO3 - Write the Verilog/VHDL coding of VLSI circuit and generate automatic test pattern. **(K3)**
CO4 - Explain algorithms for floor planning and placement of cells for optimized area and speed. **(K2)**
CO5 - Illustratethe Spartan 3E, Xilinx, Vertex FPGA devices and its specifications, I/O blocks. **(K3)**

UNIT I INTRODUCTION TO PROGRAMMABLE DEVICES (9 Hrs)

Programmable logic devices: ROM - PLA - PAL - PLD - FPGA - features, programming and applications using complex programmable logic devices; Speed performance and system programmability.

UNIT II INTRODUCTION TO ASIC (9 Hrs)

Design flow - types of ASICs - full custom with ASIC - semi custom ASICs - standard cell based ASIC - gate array based ASIC - channeled – channel less - structured - data path elements - adders - multiplier - cell compilers ; Logical effort : area and efficiency - paths - multi stage cells - optimum delay.

UNIT III LOW LEVEL DESIGN LANGUAGE (9 Hrs)

EDIF: PLA tools - introduction to CFI designs representation; Half gate ASIC: Introduction to synthesis and simulation - two level logic synthesis - high level logic synthesis - VHDL and logic synthesis - types of simulation - boundary scan test - fault simulation - automatic test pattern generation.

UNIT IV FLOOR PLANNING, PLACEMENT AND ROUTING (9 Hrs)

Physical design: CAD tools - system partitioning - estimating ASIC size - partitioning methods; Floor planning tools - I/O and power planning - clock planning - placement algorithms - iterative placement improvement; Time driven placement methods - physical design flow global routing - local routing - detail routing - special routing - circuit extraction and DRC.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Spartan 3E and Vertex Board Analysis - inputs and outputs - clock and power inputs - Xilinx I/O blocks - PLAs and PALs design using ASIC board.

Text Books

1. Smith M J S, “Application Specific Integrated Circuits”, Pearson Education, 2009.
2. Farzad N, Faranak N, “From ASICs to SOCs: A practical Approach”, Prentice Hall, 2003.
3. Wayne Wolf, "FPGA-Based System Design", Prentice Hall, 2004.

Reference Books

1. Rajsuman R, “System-on–a–Chip: Design and Test”, Artech House, 2000.
2. Farzad N, “Timing Verification of Application Specific Integrated Circuits”, 3rd Edition, Prentice Hall, 2004.
3. Digital Integrated Circuits: A Design Perspective, Jan A. Rabey, Prentice Hall of India Pvt Ltd.2009
4. Introduction to VLSI System,C. Mead & L. Canway, Addison Wesley Pub.1980
5. Basic VLSI Design: Systems and Circuits, Douglas A. Pucknell & Kamran Eshraghian, Prentice Hall of India Private Ltd., New Delhi.2006

Web Reference

1. https://www.researchgate.net/publication/331173486_Introductory_Chapter_ASIC_Technologies_and_Design_Techniques www.utdallas.edu/~zhoud/DesignEntry.
2. en.wikipedia.org/wiki/High-level_synthesis.
3. https://www.electronics-notes.com/articles/digital-embedded-processing/asic-application-specific-ic/how-to-design-asic.php.
4. https://www.engr.siu.edu/haibo/ece428/notes/ece428_intro
5. http://www.csit-sun.pub.ro/resources/asic/CH01.pdf

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	3	-
CO2	2	-	3	3	1	1	3	3	-
CO3	2	-	3	3	1	1	3	3	-
CO4	2	-	3	3	1	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VEE214 REAL TIME SYSTEMS

L	T	P	C	Hrs
3	-	-	3	45

Course Objectives

- To introduce the basic knowledge on operating systems and Microcontroller
- To Understand Multitask scheduling algorithms involved in real time systems
- To acquaint the programming language and tools
- To gain insight in the concepts on real time Databases
- To study the characteristics of real time systems

Course Outcomes

After completion of the course, the students will be able to

CO1 - Distinguish Real time operating systems and operating system. **(K3)**

CO2 - Describe multitask scheduling involved in real time systems. **(K3)**

CO3 - Explain the programming language and tools. **(K2)**

CO4 - Illustrate the concepts on real time Databases. **(K3)**

CO5 - Illustrate the characteristics of real time systems. **(K3)**

UNIT I INTRODUCTION (9 Hrs)

Introduction – Issues in Real Time Computing – Structure of a Real Time System – Task classes Performance Measures for Real Time Systems – Estimating Program Run Times – Characteristics of Real-time Systems – Classification of Real-time systems – Applications of Real-time Systems – Safety and Reliability. Basic Concepts of Scheduling: Real-time applications - Basic concepts for real-time task scheduling. Scheduling of Independent Tasks: Basic on-line algorithms for periodic tasks - Hybrid task sets scheduling.

UNIT II SCHEDULING IN REAL-TIME SYSTEMS (9 Hrs)

Scheduling of Dependent Tasks: Tasks with precedence relationships - Tasks sharing critical resources. Scheduling schemes for handling overload: Scheduling techniques in overload conditions - Handling real-time tasks with varying timing parameters - Handling overload conditions for hybrid task sets. Multiprocessor scheduling and comparison with uniprocessor scheduling

UNIT III PROGRAMMING LANGUAGE AND TOOLS (9 Hrs)

Programming Languages and Tools – Desired language characteristics – Data typing – Control structures Facilitating Hierarchical Decomposition, Packages, Run time (Exception) Error handling – Overloading and Generics – Multitasking – Low level programming – Task Scheduling – Timing Specifications

UNIT IV REAL TIME DATABASES (9 Hrs)

Real time Databases – Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two – phase Approach to improve Predictability – Maintaining Serialization Consistency – Databases for Hard Real Time Systems.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Study of operating System-Threads and Tasks-The Kernel, Time Services and Scheduling Mechanisms, other basic operating functions-Communication and Synchronization Application program interface and SSP structure

Text Books

1. Stuart Bennett, “Real-time Computer Control”, Second Edition, Pearson Education Ltd., 2012.
2. Francis Cottet, Joelle Delacroix and ZoubirMammeri, “Scheduling in Real-Time Systems”, John Wiley & Sons Ltd., 2002.
3. Liu, Jane W. S.Real-time systems Upper Saddle River, N.J.: Prentice Hall, cop. 2000.

Reference Books

1. Jane W.S.Liu- “Real Time System”- Pearson Edition-2002
2. Rajib Mall, “Real-Time Systems: Theory and Practice”, Pearson Education.TimeSys Corporation, “The Concise Handbook of Real-Time Systems”, TimeSys Corporation, Pittsburgh, PA, 2002.
3. Jane W. S. Liu, “Real Time Systems”, Pearson Education Publication, 2000
4. Mall Rajib, “Real Time Systems”, Pearson Education, 2009
5. Albert M. K. Cheng, “Real-Time Systems: Scheduling, Analysis, and Verification”, Wiley., 2002

Web References

1. nptel.ac.in/courses/106105036
2. http://www.slideshare.net/sanjivmalik/rtos-concepts
3. https://lecturenotes.in/notes/73-notes-for-real-time-systems-rts-by-lopamudra-mishra
4. http://class.ece.iastate.edu/cpre458/lecture_notes.htm
5. http://www.eecs.umich.edu/courses/eecs571/lectures/lecture1-intro

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	-	3
CO2	2	-	3	3	1	1	3	-	3
CO3	2	-	3	3	1	1	3	-	3
CO4	2	-	3	3	1	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

P20VEE215 TESTING OF VLSI CIRCUITS

L	T	P	C	Hrs
3	-	-	3	45

Course Objectives

- To introduce the basic knowledge in VLSI circuit design and to understand the fault modelling and testing
- To Understand the test generation for sequential and combinational circuits
- To acquaint the knowledge on design testability
- To gain insight in the concepts on self-test and test algorithms
- To study the concepts of fault modelling and fault identification

Course Outcomes

After completion of the course, the students will be able to

CO1 - Define VLSI circuit design, fault modelling and testing. **(K3)**
CO2 - Generate test sequence for verification of sequential and combinational circuits. **(K3)**
CO3 - Describe the concepts on design testability. **(K3)**
CO4 - Illustrate the concepts self-test and test algorithms. **(K3)**
CO5 - Simulate fault modelling algorithms. **(K4)**

UNIT I TESTING AND FAULT MODELLING (9 Hrs)

Introduction to testing – Faults in Digital Circuits – Modeling of faults – Logical Fault Models –Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation –Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION (9 Hrs)

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY (9 Hrs)

Design for Testability – Ad-hoc design – generic scan-based design – classical scan-based design.

UNIT IV SELF TEST AND TEST ALGORITHMS (9 Hrs)

Built-In self-test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test generation for Embedded RAMs.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Fault modeling – Test algorithm – Automatic test generation– Scan based design – Self test – Fault identification.

Text Books

1. A.L.Crouch, “Design Test for Digital ICs and Embedded Core Systems”, Prentice Hall International, 2002.
2. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.
3. W. W. Wen, “VLSI Test Principles and Architectures Design for Testability”, Morgan Kaufmann Publishers. 2006

Reference Books

1. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed- Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. N. Jha & S.D. Gupta, “Testing of Digital Systems”, Cambridge, 2003.
4. Michael L. Bushnell &Vishwani D. Agrawal,” Essentials of Electronic Testing for Digital, memory & Mixed signal VLSI Circuits”, Kluwar Academic Publishers. 2000.
5. S. Mourad, and Y. Zorian, "Principles of Testing Electronic Systems", John Wiley & Sons, 2000.

Web References

1. http://web.ewu.edu
2. http://ic.sjtu.edu
3. http://nptel.iitm.ac.in
4. https://lecturenotes.in/notes/9387-notes-for-vlsi-design-vlsi-by-abhishek-kumar
5. http://www.cs.uoi.gr/~tsiatouhas/CCD/Section_8_1-2p

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	3	-
CO2	2	-	3	3	1	1	3	3	-
CO3	2	-	3	3	1	1	3	3	-
CO4	2	-	3	3	1	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

PROFESSIONAL ELECTIVE – IV

Sl. No.	Course Code	Course Title	Periods			Credits	Max. Marks		
			L	T	P		CAM	ESM	Total
1	P20VEE316	VLSI Signal Processing	3	-	-	3	40	60	100
2	P20VEE317	High Speed Digital Design	3	-	-	3	40	60	100
3	P20VEE318	Real Time Operating System	3	-	-	3	40	60	100
4	P20VEE319	Soft Computing	3	-	-	3	40	60	100
5	P20VEE320	Cloud computing and Distributed System	3	-	-	3	40	60	100

P20VEE316 VLSI SIGNAL PROCESSING

L	T	P	C	Hrs
3	-	-	3	45

Course Objectives

- To describe the concepts of parallel processing in FIR filter Realization
- To Understand the concepts of systolic architecture design
- To acquire the knowledge on efficient realization of IIR filters in DSP
- To gain insight in the concepts of Finite Word Length Effect in Pipelined Architecture
- To design and simulate the FIR and IIR filters for given specification

Course Outcomes

After completion of the course, the students will be able to

CO1 - Discuss about parallel processing in FIR filter. **(K3)**

CO2 - Demonstrate the concepts of systolic architecture design. **(K3)**

CO3 - Interpret the efficient realization of IIR filters in DSP. **(K3)**

CO4 - Examine the concepts of Finite Word Length Effect in Pipelined Architecture. **(K3)**

CO5 - Design FIR and IIR filters for given specification. **(K4)**

UNIT 1 PARALLEL PROCESSING IN FIR FILTER REALIZATION (9 Hrs)

DSP systems, Programs, Applications, Representation, Data flow graphs, Loop Bound and Iteration Bound, Algorithms, Iteration Bound of Multirate Data-flow graphs, Pipelining of FIR filters, Parallel Processing of FIR filters.

UNIT II SYSTOLIC ARCHITECTURE DESIGN (9 Hrs)

Retiming – properties, applications, Solving inequality systems, Retiming techniques, Unfolding-algorithm, application, properties, Critical path, Folding transformation, Techniques, Folded architectures, Folding of Multirate systems, Systolic architecture design methodology, FIR systolic arrays, Scheduling vector, Matrix-Matrix multiplication, Systolic design for space representations with delays

UNIT III EFFICIENT REALIZATION OF IIR FILTERS IN DSP (9 Hrs)

Fast convolution algorithms, Iterated, Cyclic Convolutions, Design by Inspection, DCT and Inverse DCT, Parallel architectures for rank -order filters, Pipeline interleaving in digital filters, Pipelining in 1^{st}-order and higher-order IIR Digital Filters, Parallel processing for IIR Filters, Combined pipelining and parallel processing for IIR Filters.

UNIT IV FINITE WORD LENGTH EFFECT IN PIPELINED ARCHITECTURE (9 Hrs)

Scaling and Round off noise, State variable description, Scaling and Round-off noise computation, Round off noise in pipelined IIR filters, Round off noise computation using state variable, Slow-Down, Retiming, and Pipelining, Fast binary adders and multipliers, Parallel multipliers.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Design and simulate FIR and IIR filters for the given specifications study of finite word length effect in different realization

Text Books

1. K K. Parhi, “VLSI Digital Signal Processing Systems: Design and Implementation”, Wiley, 2009
2. M. Ismail and T. Fiez, “Analog VLSI: Signal and Information Processing”, McGraw-Hill, 2004
3. U. Meyer, Baese, *Digital Signal Processing with Field Programmable Gate Arrays*, Springer, Second Edition, 2004

.

Reference Books

1. Kowshik Roy “Low Power CMOS VLSI Circuit Design” Wiley, 2000
2. Keshab K. Parhi, *VLSI* Digital Signal Processing Systems, Design and implementation, Wiley, Interscience, 2007.
3. Neil H.E. Weste and Kamran Eshraghian, „Principles of CMOS VLSI Design‟, Pearson Education ASIA, 2nd edition, 2000.
4. Keshab K. Parhi. VLSI Digital Signal Processing Systems, Wiley-Inter Sciences, 2006
5. Jose E. France, YannisTsividls, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing’ Prentice Hall, 2004.

Web References

1. http:// www.nptel.iitm.ac.in
2. www.aticourses.com/Advanced%20Topics%20in%20Digital%20Signals
3. https://www.stuvia.com/doc/323898/vlsi-signal-processing-important-notes
4. https://www.win.tue.nl/~wsinmak/Education/2IMN35/2IMN35-2016-slides1
5. https://sites.google.com/site/personalwebpageofprofsuresh/subjects-handled/vlsi-signal-processing

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	3	-
CO2	2	-	3	3	1	1	3	3	-
CO3	2	-	3	3	1	1	3	3	-
CO4	2	-	3	3	1	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VEE317 HIGH SPEED DIGITAL DESIGN

L	T	P	C	Hrs
3	-	-	3	45

Course Objectives

- To introduce the basic digital design and transmission concepts
- To study the working principle of power distribution
- To gain insight to the working of signalling circuits
- To acquaint the various characteristic of timing convention and synchronization
- To study the characteristics of transmission lines

Course Outcomes

After completion of the course, the students will be able to

CO1 - Explain the basic transmission concepts. **(K2)**
CO2 - Relate power distribution and noise. **(K3)**
CO3 - Describe the working of signalling circuits. **(K3)**
CO4 - Illustrate the characteristic of timing convention and synchronization. **(K3)**
CO5 - Simulate and infer ISI. **(K4)**

UNIT I INTRODUCTION (9 Hrs)

Frequency, time and distance - Capacitance and Inductance Effects - High speed properties of logical gates - Speed and power modeling of wires -Geometry and Electrical properties of wires - Electrical model of Transmission lines - Lossless LC transmission lines - Lossy RLC transmission lines – Special transmission lines.

UNIT II POWER DISTRIBUTION AND NOISE (9 Hrs)

Power supply network - Local power regulation IR drops Area bonding - On chip bypass capacitors, Power supply isolation– Noise sources in digital system, Power supply Noise – Cross talk, Inter-symbol interference.

UNIT III SIGNALING CONVENTION AND CIRCUITS (9 Hrs)

Signaling modes for transmission lines- Signaling over lumped transmission media, Signaling over RC interconnects, driving lossy LC lines- Terminators, transmitter and receiver circuits.

UNIT IV TIMING CONVENTION AND SYNCHRONIZATION (9 Hrs)

Timing fundamentals -Timing properties of clocked storage elements -Signals and events, Open loop Timing -Level sensitive clocking - Pipeline timing - Closed loop Timing – Clock Distribution, Synchronization failure – Electromagnetic Compatibility.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Study the characteristics of Transmission lines – Noise sources – ISI by simulation and measure ISI by CRO.

Text Books

1. WilliamS.Dally& John W. Paulton, Digital System Engineering, Cambridge University Press, 2008.
2. Masakazu Shoji, High Speed Digital Circuits, Addison Wesley Publishing Company, 2004.
3. S. Hall, G. Hall, and J. McCall, High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley-Interscience, 2000.

Reference Books

1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic; “Digital Integrated Circuits: A design Perspective”, 2nd Edition PHI, 2003.
2. Paul CR, "Introduction t Electromagnetic compatibility", Wiley 2006.
3. Gelyer, Allen, Strider, “VLSI Design techniques for analog & digital circuits”, McGraw Hill, 2008.
4. Howard Johnson & Martin Graham, “High Speed Digital Design” A Handbook of Black Magic, Prentice Hall PTR, 2009.
5. Goel A K, "High speed VLSI interconnections", Wiley 2007

Web References

1. http://www-cad.eecs.berkeley.edu/Software/software.html
2. www.synopsys.com/products/ mixed signal/hspice/hspice.html
3. http://blackboard.jhu.edu
4. http://www.specctraquest.com
5. http://electronix.org.ru/books/high-speed-digital-desig

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	3	-
CO2	2	-	3	3	1	1	3	3	-
CO3	2	-	3	3	1	1	3	3	-
CO4	2	-	3	3	1	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VEE318 REAL TIME OPERATING SYSTEM

L	T	P	C	Hrs
3	-	-	3	45

Course Objectives

- To introduce the basic knowledge on Computer Programming, microcontroller-based system and embedded system
- To Understand the concepts on Structure of RTOS µCOS / Embedded Linux and interaction of OS with a computer and application development using RTOS
- To acquaint the knowledge on Synchronization & Communication in µCOS-II / Embedded Linux
- To gain insight in the concepts of Process Management, I/O, Memory Management in RTOS
- To Design and simulate static and dynamic scheduling and WINCE

Course Outcomes

After completion of the course, the students will be able to

CO1 - Explain Computer Programming and Microcontroller based System. **(K2)**

CO2 - Describe the concepts on Structure of RTOS µCOS / Embedded Linux. **(K2)**

CO3 - Describe the knowledge on Synchronization & Communication in µCOS-II / Embedded Linux. **(K2)**

CO4 - Illustrate the concepts of Process Management, I/O, Memory Management in RTOS. **(K3)**

CO5 - Simulate various scheduling algorithm. **(K4)**

UNIT I STRUCTURE OF RTOS µCOS / EMBEDDED LINUX (9 Hrs)

RTOS features, Resources and shared resources Task, Task control block. Task scheduling. Task level context switching, Syntax related to Context switching, Locking and unlocking of scheduler, Idle & Static task, Interrupt under RTOS, ISR under RTOS, Servicing an interrupt, Clock Tick. Initialization and Starting the RTOS, Multitasking, Task Management function, Event Control Blocks, Task State Management.

UNIT II SYNCHRONIZATION & COMMUNICATION IN µCOS-II / EMBEDDED LINUX (9 Hrs)

Semaphore management Functions with µCOS-II / Embedded Linux API, ECB as Semaphore, Mutual exclusion Semaphore functions, Event Flag management Functions, Mailbox management, ECB As Mailbox, Message Queue management, ECB as Message Queue, Message Queue Management Function.

UNIT III PROCESS, I/O, MEMORY MANAGEMENT IN RTOS (9 Hrs)

Process Management, Timer functions, Device, File, I/O subsytems management, Memory Management, Memory Control Block, Dynamic memory allocation.

UNIT IV WinCE (9 Hrs)

Introduction WinCE, Polled Loop Systems – RTOS Porting to a Target, Explanation of Application, Kernel, OAL, Explanation of CPU, SOC, Platform, MMU, MMU for ARM based devices in WinCE, Overview of Boot loader, eboot Directory Structure, Implementing Startup Code. Comparison study of µCos-II, Embedded Linux, Real Time Linux, Vx-Works, QNX Nutrino, ThreadEX.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Design and simulate static and dynamic scheduling algorithms in suitable platform. Study of RTOS used for Washing Machine, Air Conditioner, Microwave Oven, Engine Management System using CAN, Automatic Chocolate Vending Machine

Text Books

1. Samuel Phuns, Professional Windows Embedded CE 6.0, Wrox, 2008.
2. D.M.Dhamdhere," Operating Systems,A Concept-Based Approch,TMH,2008
3. SriramIyer, Pankaj Gupta, Embedded Real time Systems Programming, Tata McGraw Hill Publishing Company Limited, 2004.

Reference Books

1. Silberschatz, Galvin,Gagne, " Operating System Concepts,6thed,John Wiley,2003
2. Rajkamal, Embedded System, Tata McGraw Hill, 2003.
3. Dreamtech Software Team, Programming for Embedded Systems, Wiley Publishing Inc., 2003.
4. Qing Li, "Real Time Concepts for Embedded Systems", Elsevier, 2011,
5. Dr. Craig Hollabaugh, "Embedded Linux: Hardware, Software and Interfacing", 1st Edition, Pearson, 2008.

Web References

1. http:// www.nptel.iitm.ac.in
2. http://www.ocw.mit.edu.
3. http://web.iiit.ac.in/~bezawada/CN.html
4. https://www.tutorialspoint.com/Real-Time-Embedded-Systems
5. https://www.engineersgarage.com/article_page/rtos-real-time-operating-system/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	-	2
CO2	2	-	3	3	1	1	3	-	2
CO3	2	-	3	3	1	1	3	-	2
CO4	2	-	3	3	1	1	3	-	2
CO5	2	2	3	3	2	1	3	-	2

P20VEE319 SOFT COMPUTING

L	T	P	C	Hrs
3	-	-	3	45

Course Objectives

- To understand the fundamental theory and concepts of neural networks, neuro-modeling, several neural network paradigms and its applications.
- To introduce the fuzzy logic concepts, fuzzy principles and relations.
- To learn about genetic algorithm implementation in soft computing.
- To embed fuzzy logic with genetic algorithms for computing.
- To understand different soft computing tools to solve real life problems.

Course Outcomes

After completion of the course, the students will be able to

CO1 -Explain the fundamental theory and concepts of neural networks, Identify different neural network architectures, algorithms, applications and their limitations. **(K2)**

CO2 - Apply fuzzy logic and reasoning to handle uncertainty and solve engineering problems. **(K3)**

CO3 - Apply genetic algorithms to combinatorial optimization problems. **(K3)**

CO4 - Design hybrid system to revise the principles of soft computing in various applications. **(K3)**

CO5 - Apply modern software tools to solve real problems using a soft computing approach and evaluate various soft computing approaches for a given problem. **(K3)**

UNIT I NEURAL NETWORK (9 Hrs)

Basic concept - mathematical model - properties of neural networks - architectures - different learning methods - common activation functions - application of neural networks; Neuron architecture: Algorithms - McCullo h-Pitts - Back propagation NN - ADALINE - MADALINE - Discrete Hopfield net - BAM - Maxnet..

UNIT II FUZZY SETS & LOGIC (9 Hrs)

Fuzzy versus Crisp - fuzzy sets - fuzzy relations - laws of propositional logic - inference - Predicate logic fuzzy logic - quantifiers - inference - defuzzification methods.

UNIT III GENETIC ALGORITHM (9 Hrs)

Role of GA - fitness function - selection of initial population - cross over (different types) - mutation - inversion - deletion - constraints handling and applications of travelling salesman and graph coloring.

UNIT IV HYBRID SYSTEMS (9 Hrs)

Hybrid Systems: GA based BPNN (Weight determination) - Neuro fuzzy systems - Fuzzy BPNN - fuzzy neuron - architecture - learning - Fuzzy logic controlled genetic algorithm

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Simulation of PSD - HSA and ACO related to either wireless networking or Antenna or Image Processing using related tools.

Text Books

1. S.N. Sivanandam, S.N. Deepa, “Principles of Soft Computing”, 2nd Edition, John Wiley India, 2012.
2. S. Haykin, “Neural Networks - A Comprehensive Foundation”, 2nd Edition, Pearson Education, 2005.
3. T.S. Rajasekaran, G.A. VijaylakshmiPai, “Neural Networks, Fuzzy Logic & Genetic Algorithms – Synthesis and Applications”, Prentice-Hall India, 2003.

Reference Books

1. Goldberg David, “Genetic Algorithms”, Pearson Education, 2006.
2. J.-S. R. Jang, C.-T. Sun, and E. Mizutani , “Neuro-Fuzzy and soft Computing” , PHI Learning, 2009.
3. Simon Haykin, “Neural Networks and Learning Machines”, 3rd edition, PHI Learning, 2011.
4. Timothy J. Ross,” Fuzzy Logic with Engineering Applications”, 3rd Edn., Willey, 2010.
5. David E. Goldberg, Genetic Algorithm in Search Optimization and Machine Learning Pearson Education India, 2013

Web References

1. http://www.vssut.ac.in/lecture_notes/lecture1423723637.pdf
2. https://lecturenotes.in/subject/124/soft-computing-sc
3. https://nptel.ac.in/courses/106/105/106105173/
4. https://sites.google.com/site/7csesoftcomputing/course/lecture-note
5. https://www.tutorialspoint.com/fuzzy_logic/index.htm

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	-	2
CO2	2	-	3	3	1	1	3	-	2
CO3	2	-	3	3	1	1	3	-	2
CO4	2	-	3	3	1	1	3	-	2
CO5	2	2	3	3	2	1	3	-	2

P20VEE320	CLOUD COMPUTING AND DISTRIBUTED SYSTEMS	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To understand Cloud computing fundamentals and architecture
- To know about various cloud-based web services
- To introduce into technologies and tools for cloud computing
- To learn about various cloud service environments
- To study and apply the knowledge of cloud services

Course Outcomes

After completion of the course, the students will be able to

CO1 - Identify the architecture and infrastructure of cloud computing and explain the core issues of cloud computing such as security, privacy, and interoperability. **(K3)**

CO2 - Explain recent research results in cloud computing and identify their pros and cons. **(K2)**

CO3 - Implement Cloud computing and deployment techniques. **(K3)**

CO4 - Deploy applications over commercial cloud computing infrastructures such as Amazon Web Services, Windows Azure, and Google App Engine. **(K3)**

CO5 - Solve a real-world problem using cloud computing through group collaboration. **(K4)**

UNIT I CLOUD COMPUTING FUNDAMENTALS (9 Hrs)

Cloud Computing definition, private, public and hybrid cloud. Cloud types; IaaS, PaaS, SaaS. Benefits and challenges of cloud computing, public vs private clouds, role of virtualization in enabling the cloud; Business Agility: Benefits and challenges to Cloud architecture. Application availability, performance, security and disaster recovery; next generation Cloud Applications

UNIT II CLOUD APPLICATIONS (9 Hrs)

Technologies and the processes required when deploying web services; Deploying a web service from inside and outside a cloud architecture, advantages and disadvantages.

UNIT III MANAGEMENT OF CLOUD SERVICES (9 Hrs)

Reliability, availability and security of services deployed from the cloud. Performance and scalability of services, tools and technologies used to manage cloud services deployment; Cloud Economics: Cloud Computing infrastructures available for implementing cloud-based services.

UNIT IV APPLICATION DEVELOPMENT (9 Hrs)

Service creation environments to develop cloud-based applications. Development environments for service development; Amazon, Azure, Google App

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Analysis of Case Studies when deciding to adopt cloud computing architecture. How to decide if the cloud is right for your requirements. Cloud based service, applications and development platform deployment so as to improve the total cost of ownership (TCO).

Text Books

1. Gautam Shroff, “Enterprise Cloud Computing Technology Architecture Applications”, Cambridge University Press; 1st edition, 2010.
2. Toby Velte, Anthony Velte, Robert Elsen peter,“Cloud Computing, A Practical Approach” McGraw-Hill Osborne Media; 1stedition , 2009
3. Dimitris N. Chorafas, “Cloud Computing Strategies” CRC Press; 1st edition,2010

Reference Books

1. Thomas Erl , Ricardo Puttini , Zaigham Mahmood , “Cloud Computing : Concepts, Technology & Architecture”, Pearson Education (US),2013.
2. Frank M. Groom, Stephan S. Jones,”Enterprise Cloud Computing for Non-Engineers”, Taylor & Francis Ltd, CRC Press, 2018
3. Zaigham Mahmood , Richard Hill, ”Cloud Computing for Enterprise Architectures”, Springer London Ltd, 2014
4. K. Hwang, G. Fox and J. Dongarra, Distributed and Cloud Computing Morgan Kaufmann Publishers, 2012.
5. Rajkumar Buyya James Broberg, Andrzej,” Cloud Computing Principles and Paradigms”, M.Goscinski Wile, 2011.

Web References

1. https://www.iare.ac.in/sites/default/files/lecture_notes/CC%20LECTURE%20NOTES.pdf
2. https://nptel.ac.in/courses/106/105/106105167/
3. https://mrcet.com/pdf/Lab%20Manuals/IT/R15A0529_CloudComputing_Notes-converted.pdf
4. https://mrcet.com/downloads/digital_notes/CSE/IV%20Year/CLOUD%20COMPUTING%20NOTES.pdf
5. https://nptel.ac.in/courses/106/106/106106107/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	2	1	2	-	2
CO2	2	-	3	3	2	1	2	-	2
CO3	2	-	3	3	2	1	2	-	2
CO4	2	-	3	3	2	1	2	-	2
CO5	2	2	3	3	2	1	2	-	2

PROFESSIONAL ELECTIVE – V

Sl. No.	Course Code	Course Title	Periods			Credits	Max. Marks		
			L	T	P		CAM	ESM	Total
1	P20VEE321	Advanced Embedded System	3	-	-	3	40	60	100
2	P20VEE322	Advanced Image Processing	3	-	-	3	40	60	100
3	P20VEE323	Hardware Software Co-Design	3	-	-	3	40	60	100
4	P20VEE324	Micro-Electromechanical Systems	3	-	-	3	40	60	100
5	P20VEE325	Nano Electronics	3	-	-	3	40	60	100

P20VEE321	ADVANCED EMBEDDED SYSTEM	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To get introduced into basic building blocks of embedded system
- To familiarize with the architecture and partitioning of embedded system
- To understand about the matching of hardware and software in a system
- To understand memory and I/O interfacing
- To apply the embedded knowledge in processor design

Course Outcomes

After completion of the course, the students will be able to

CO1 - Describe the timing and interrupt in processor. **(K2)**

CO2 - Apply co design methodology. **(K3)**

CO3 - Solve the Co-Synthesis Problem in embedded field. **(K3)**

CO4 - Explain the memories and communication protocol in embedded field. **(K2)**

CO5 - Design a simple processor model. **(K4)**

UNIT I INTRODUCTION TO EMBEDDED HARDWARE AND SOFTWARE (9 Hrs)

Terminology – Gates – Timing diagram – Memory – Microprocessor buses – Direct memory access – Interrupts – Built interrupts – Interrupts basis – Shared data problems – Interrupt latency - Embedded system evolution trends – Interrupt routines in an RTOS environment.

UNIT II SYSTEM MODELING WITH HARDWARE/SOFTWARE PARTITIONING (9 Hrs)

Embedded systems, Hardware/Software Co-Design, Co-Design for System Specification and modeling-Single-processor Architectures &,Multi-Processor Architectures, comparison of Co Design Approaches, Models of Computation, Requirements for Embedded System Specification, Hardware/Software Partitioning Problem, Hardware/Software Cost Estimation, Generation of Partitioning by Graphical modeling, Formulation of the HW/SW scheduling, Optimization.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS (9 Hrs)

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV MEMORY AND INTERFACING (9 Hrs)

Memory: Memory write ability and storage performance – Memory types – composing memory – Advance RAM interfacing communication basic – Microprocessor interfacing I/O addressing – Interrupts – Direct memory access – Arbitration multilevel bus architecture – Serial protocol – Parallel protocols – Wireless protocols – Digital camera example

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Design Process Model- Embedded System modeling with Hardware/Software Partitioning. Develop a model arbitration multilevel bus architecture and digital camera.

Text Books

1. David. E. Simon, “An Embedded Software Primer”, Pearson Education, 2012.
2. Tammy Noergaard,” Embedded System Architecture, A comprehensive Guide for Engineers and Programmers”, Elsevier, 2008
3. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2012.

Reference Books

1. Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & sons, 2014.
2. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.
3. Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design” Kaufmann Publishers, 2001
4. Youn-long, Steve Lin, “Essential issues of SoC design”, Springer – 2006.
5. Glaf P.Feiffer, Andrew Ayre and Christian Keyold, “Embedded Networking with CAN and CAN open”, Embedded System Academy 2005.

Web References

1. www.vectorindia.org/embedded_coursecontent.html
2. www.cetpainfotech.com
3. http://nptel.ac.in/courses/117106030/35
4. https://link.springer.com
5. http://www.can-cia.org/can/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	-	3
CO2	2	-	3	3	1	1	3	-	3
CO3	2	-	3	3	1	1	3	-	3
CO4	2	-	3	3	1	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

P20VEE322	ADVANCED IMAGE PROCESSING	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To learn about the basic concepts of digital image processing
- To understand the importance of image segmentation and estimation techniques
- To familiarize in various image compression techniques
- To introduce into image security and image forensic concepts
- To apply simulation tool to analyse real life image

Course Outcomes

After completion of the course, the students will be able to

CO1 - Demonstrate the fundamental concepts of a digital image processing system. **(K3)**

CO2 - Estimate the digital image by various techniques. **(K3)**

CO3 - Categorize and interpret various compression techniques. **(K3)**

CO4 - Differentiate and analyze the methods used for image security and forensics. **(K3)**

CO5 -Simulate an image for forensic analysis. **(K4)**

UNIT I DIGITAL IMAGE FUNDAMENTALS (9 Hrs)

Image fundamentals: Image acquisition - sampling and quantization - image resolution- basic relationship between pixels - colour images - RGB, HSI and other models; Transform based models (DFT, DCT, DWT); Image Enhancement: Spatial and frequency averaging - smoothening and sharpening filters.

UNIT II SEGMENTATION AND DENOISING (9 Hrs)

Image Segmentation: Edge detection - edge linking via Hough transform - thresholding- region based segmentation; Denoising: Maximum likelihood estimation - Bayesian estimators - model selection (MDL principle) - transform based denoising - adaptive wiener filtering - soft shrinkage and hard thresholding.

UNIT III IMAGE COMPRESSION (9 Hrs)

Image compression: Basics of source coding theory (lossless and lossy) - Vector quantization - codebook design - transform and sub band coding.

UNIT IV IMAGE SECURITY AND FORENSIC (9 Hrs)

Image Security: cryptography and steganography techniques- Chaos based and Non-Chaos based methods; Image Forensics: Key photographic techniques-detection techniques for crime scene analysis

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Simulation of preprocessing techniques-implementation of image processing techniques for real time applications-forensic analysis using related tools.

Text Books

1. Rafael C Gonzalez and Richard E Woods, “Digital Image Processing”, 2nd Edition, Pearson Education, 2004.
2. Anil K Jain, “Fundamentals of Digital Image Processing”, 3rd Edition, Pearson Education, 2002.
3. William K Pratt, “Digital Image Processing”, 2nd Edition, John Wiley, 2002.

Reference Books

1. Parekh R, “Principles of Multimedia”, Tata McGraw-Hill, 2006.
2. Robinson and Edward, “Introduction to Crime Scene Photography”, Elsevier/Academia Press, 2012.
3. Herbert Blitzer, Karen Stein-Ferguson and Jeffrey Huang, “Understanding Forensic Digital Imaging”, 1st edition, Academic Press, 2008.
4. Prabat K Andleigh and KiranThakrar, “Multimedia Systems and Design”, Prentice Hall India, 2007.
5. Tay Vaughan, “Multimedia Making It Work”, McGraw Hill, 2011

Web References

1. www.imageprocessingplace.com/DIP-3E/dip3e_main_page.html
2. https://www.tutorialspoint.com/dip/
3. https://homepages.inf.ed.ac.uk/rbf/HIPR2/glossary.htm
4. https://www.coursera.org/courses?query=image%20processing
5. https://www.edx.org/learn/image-processing

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	-	2
CO2	2	-	3	3	1	1	3	-	2
CO3	2	-	3	3	1	1	3	-	2
CO4	2	-	3	3	1	1	3	-	2
CO5	2	2	3	3	2	1	3	-	2

P20VEE323	HARDWARE SOFTWARE CO-DESIGN	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To acquire the knowledge about system specification and modeling
- To learn the formulation of partitioning the hardware and software
- To analyze about the hardware and software integration
- To learn about target architecture and its related systems
- To learn about Xilinx tool for synthesis

Course Outcomes

After completion of the course, the students will be able to

CO1 - Demonstrate about system specification and modelling. **(K3)**

CO2 - Differentiate and analyse the partition needed for hardware/software. **(K3)**

CO3 - Analyse the hardware and software integration problem for implementation of distributed system. **(K4)**

CO4 - Categorize the prototype and emulation needed for the system based on application. **(K4)**

CO5 - Integrate hardware processor with IP. **(K4)**

UNIT I SYSTEM SPECIFICATION AND MODELING (9 Hrs)

Embedded Systems , Hardware/Software Co-Design , Co-Design for System Specification and Modelling, Co-Design for Heterogeneous Implementation - Processor Synthesis , Single-Processor Architectures with one ASIC , Single-Processor Architectures with many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches , Models of Computation ,Requirements for Embedded System Specification.

UNIT II HARDWARE/SOFTWARE PARTITIONING (9 Hrs)

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS (9 Hrs)

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis.

UNIT IV PROTOTYPING AND EMULATION (9 Hrs)

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture- Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Design a System Level Synthesis, by learning the basics of the Xilinx Vivado High Level Synthesis (HLS) CAD Flow: Design Entry, Compiling, and Simulation. Create a complete Hardware/Software Co-design that integrates the Arm Processor with an IP.

Text Books

1. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”,Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup, Wayne Wolf,” Hardware/Software Co-Design: Principles and Practice”, Kluwer Academic Pub,1997.
3. Giovanni De Michele, Rolf Ernst Morgon,” Reading in Hardware/Software Co-Design “Kaufmann Publishers,2001.

Reference Books

1. Joris van den Hurk , Jochen A.G. Jess," System Level Hardware/Software Co-Design : An Industrial Approach", Springer-Verlag New York Inc., 2010
2. Jean-Michel Berge , Oz Levia , Jacques Rouillard,"Hardware/Software Co-Design and Co-Verification", Springer-Verlag New York Inc., 2010
3. RuiruiGu , Shuvra S Bhattacharyya , William S Levine" Hardware Software Co-Design for Parallel Embedded Systems", LAP Lambert Academic Publishing, 2011
4. Sao-Jie Chen , Guang-Huei Lin , Pao-Ann Hsiung , Yu Hen Hu," Hardware Software Co-Design of a Multimedia SOC Platform", Springer,2010.
5. Patrick Schaumont "A Practical Introduction to Hardware/Software Co-design", Patrick Schaumont, Springer, 2012.

Web References

1. https://www.cs.ccu.edu.tw/~pahsiung/.../notes/SoC_Design_Flow_Tools_Codesign.pdf
2. http://faculty.cs.tamu.edu/rabi/cpsc689/lectures/lecture01/Introduction_to_codesign.pdf
3. https://iit.uloop.com/course-notes/1154-ECE/864975-ECE-587-HardwareSoftware-Codesign
4. https://semiengineering.com/hardware-software-co-design-reappears/
5. https://www.cs.ccu.edu.tw/~pahsiung/courses/codesign/resources/tutorials.html

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	-	1
CO2	2	-	3	3	1	1	3	-	1
CO3	2	-	3	3	1	1	3	-	1
CO4	2	-	3	3	1	1	3	-	1
CO5	2	2	3	3	2	1	3	-	1

P20VEE324	MICRO-ELECTROMECHANICAL SYSTEMS	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To introduce into the MEMS technology
- To provide knowledge of semiconductors and solid mechanics to fabricate MEMS devices
- To introduce various sensors and actuators
- To introduce different materials used for MEMS
- To educate on the applications of MEMS to disciplines beyond Electrical and Mechanical engineering

Course Outcomes

After completion of the course, the students will be able to

CO1 - Demonstrate the MEMS technology with its mathematical characterization. **(K3)**
CO2 - Analyse the recent research trends in fabrication process of MEMS technology. **(K3)**
CO3 - Recognize and apply the type of sensor needed based on applications. **(K3)**
CO4 - Analyse and design the RF filters used for MEMS technology. **(K4)**
CO5 - Simulate the devices needed for MEMS implementation. **(K4)**

UNIT I INTRODUCTION TO MEMS (9 Hrs)

Evolution of Micro Electromechanical Systems (MEMS): Driving force for MEMS development - MEMS material properties - microelectronics technology for MEMS; The Finite Element Method: Important mathematical and physical concept in FEM - discretization and other approximation.

UNIT II MICROMACHINING Technology for MEMS (9 Hrs)

Fabrication Process: MEMS fabrication technologies - bulk micro machining - surface micro machining - LIGA process; Bonding and packing of MEMS - MEMS reliability - scaling in MEMS; Recent research direction in MEMS: CMOS- MEMS integration - polymer MEMS - NEMS etc.

UNIT III SENSOR AND ACTUATORS (9 Hrs)

Sensors: Classifications - principle - design and characterization of thermal – micromachined -mechanical - pressure - flow sensor - bio– sensor; Actuation in MEMS Devices: Electrostatic actuation - parallel plate capacitor - cantilever beam-based movement; MEMS accelerometers; optical MEMS: Micro mirror.

UNIT IV RF MEMS (9 Hrs)

Switches: Cantilever MEMS based switch; Inductors and Capacitors: Modeling and design issues of planar inductor and capacitors; RF Filters: Modeling of mechanical filters; Phase Shifters: Classifications and limitations; Micro Machined Antennas: Micro-strip antennas - design parameters

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Modeling, simulation and analysis in the applications of MEMS switch, sensors and actuators using related platform.

Text Books

1. Madou M, “Fundamentals of Micro Fabrication” CRC Press, 3rd Edition, 2011.
2. Senturia, “Micro System Design”, Kluwer, 2007.
3. Maluf N, Williams K “An Introduction to Micro- electromechanical Systems Engineering” Artech House, 2nd Edition, 2004.

Reference Books

1. Rebeiz G, “RF MEMS: Theory, Design, and Technology” Wiley/ IEEE Press, 2004.
2. Varadan V K, Vinoy K J, Jose K A, “RF MEMS and Their Applications” Wiley & Sons, 2003.
3. James J.Allen, “Micro Electro Mechanical System Design”, CRC Press Publisher, 2010
4. Thomas M.Adams and Richard A.Layton, Introduction MEMS, Fabrication and Application, Springer 2012.
5. Chang Liu, “Foundations of MEMS”, Pearson Education Inc., 2006.

Web References

1. http://freevideolectures.com/blog/2010/11/130-nptel-iit-online-courses/#
2. http://biomedikal.in/2011/02/lecture-notes-on-mems-technology/
3. http://www.learnerstv.com/Free-engineering-Video-lectures-ltv122-Page1.html
4. https://lecturenotes.in/notes/16712-note-for-microelectromechanical-systems-mems-by-abhishek-apoorv
5. https://nptel.ac.in/courses/117/105/117105082/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	-	1
CO2	2	-	3	3	-	1	3	-	1
CO3	2	-	3	3	-	1	3	-	1
CO4	2	-	3	3	-	1	3	-	1
CO5	2	2	3	3	2	1	3	-	1

P20VEE325 NANO ELECTRONICS

L	T	P	C	Hrs
3	-	-	3	45

Course Objectives

- To learn the basic concepts of nano electronics.
- To understand working of nano scale CMOS transistor.
- To understand modelling aspects of nano scale devices from perspective of circuit applications.
- To provide knowledge of nano electronics memories and its applications.
- To know the concepts of lithography and its types.

Course Outcomes

After completion of the course, the students are able to

CO1 - Explain the concepts of nano electronics. **(K2)**
CO2 - Building molecular level devices and systems. **(K3)**
CO3 - Design of Carbon based Nanoelectronic devices. **(K3)**
CO4 - Summarize the types and applications of nano electronic memories. **(K3)**
CO5 - Summarize concepts and classifications of lithography. **(K4)**

UNIT I INTRODUCTION (9 Hrs)

Particles, waves, Wave mechanics, schrodinger equation, free and confined electrons, particle statistics and density of states. Electron transport in semiconductors and nanostructures, Quantum dots, Quantum Well, Quantum wire, materials and its properties, Ballistic electron transport, 1D transport, Spin electronics- Electrical and Electronics Applications of Nanotechnology.

UNIT II NANOSCALE CMOS (9 Hrs)

Survey of modern electronics and trends towards nano electronics CMOS scaling, challenges and limits, static power, device variability, interconnect - CNT-FET, HEMT, pHEMTF in FET, Ferro FET nanoscale CMOS circuit design and analysis.

UNIT III NANOELECTRONIC STRUCTURE AND DEVICES (9 Hrs)

Resonant-tunneling diodes- Resonant Tunneling Transistor-Single-electron transfer devices- Potential effect transistors- Quantum-dot cellular automata, Nano Photonic Devices-Molecular electronic devices -Nano-electromechanical system devices.

UNIT IV NANOELECTRONIC MEMORIES (9 Hrs)

Nano tube for memories- Nano RAM- Nanoscale DRAM, SRAM, Tunnel magneto resistance-Giant magneto resistance- design and applications.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Assignment and presentation on Nanolithography-Importance of micro/nano patterning-Classification of lithographic techniques-Photolithography – A conventional and classical method -Ion beam Lithography -X-ray lithography -Electron beam lithography-Alternate Nanolithographic Techniques.

Text Books

1. George W. Hanson, Fundamental of Nanoelectronics, Pearson education.2008.
2. Adrian Ionesu and Kaustav Banerjee eds. “Emerging Nanoelectronics: Life withand after CMOS”, Vol I, II, and III, Kluwer Academic, 2005.
3. W.R. Fahrner, Nanotechnology and Nanoelctronics, Springer, 2005.

Reference Books

1. Michael A. Nielsen and Isaac L. Chuang, “Quantum Computation and Quantum Information”, Cambridge University Press, 2000.
2. Kiyoo Itoh Masashi Horiguchi, Hitoshi Tanaka, Ultra Low voltage nano scale memories. Spl Indian Edition, Springer.
3. V. Mitin, V. Kochelap, and M. Stroscio “Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications”, Cambridge University Press, 2008.
4. S. Datta, “Lessons from Nanoelectronics: A New Perspective on Transport (Lessons from Nanoscience: a Lecture Notes Series) World Scientific, 2012

5. Chattopadhyay, Banerjee, Introduction to Nanoscience & Technology, PHI, 2012

Web Reference

1. onlinelibrary.wiley.com › Materials Science › Analysis/Characterization of nano systems.
2. https://www.fisgeo.unipg.it/~luca.../fisinfo/.../Electronics-beyond-nanoscale cmo
3. https://nptel.ac.in/courses/117/108/117108047/
4. https://www.nanowerk.com/nanoelectronics.php
5. https://www.mitre.org/sites/default/files/pdf/nano_overview.

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	1	3	-	1
CO2	2	-	3	3	-	1	3	-	1
CO3	2	-	3	3	-	1	3	-	1
CO4	2	-	3	3	-	1	3	-	1
CO5	2	2	3	3	2	1	3	-	1

PROFESSIONAL ELECTIVE – VI

Sl. No.	Course Code	Course Title	Periods			Credits	Max. Marks		
			L	T	P		CAM	ESM	Total
1	P20VEE326	Pervasive Devices and Technology	3	-	-	3	40	60	100
2	P20VEE327	Robotics and Automation	3	-	-	3	40	60	100
3	P20VEE328	System-on-Chip Design	3	-	-	3	40	60	100
4	P20VEE329	VLSI for Wireless Communication	3	-	-	3	40	60	100
5	P20VEE330	RISC Processor Architecture and Programming	3	-	-	3	40	60	100

P20VEE326	PERVASIVE DEVICES AND TECHNOLOGY	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To know the concepts of mobile computing
- To study the pervasive networking and web-based applications
- To learn the pervasive computing devices and its applications
- To expose the security and privacy issues in mobile computing
- To learn the technical, economic and service advantages of next generation networks

Course Outcomes

After completion of the course, the students are able to

CO1 - Explain the basic concepts of mobile computing. **(K2)**

CO2 - Describe pervasive networking and web applications. **(K2)**

CO3 - Design and develop a pervasive computing device for a specific need. **(K3)**

CO4 - Develop an attitude to identify and propose solutions for security and privacy issues. **(K3)**

CO5 - Design and deploy wireless sensor networks for specific applications. **(K4)**

UNIT I INTRODUCTION (9 Hrs)

Ubiquitous or Pervasive Computing – Context – Definitions and types Context – aware Computing and Applications -Mobile computing - Networks- Middleware and gateways - Applications and services- Developing mobile computing applications- Architecture for mobile computing - Design considerations for mobile computing.

UNIT II PERVASIVE NETWORKING (9 Hrs)

Introduction, Networking Infrastructure and Architecture of PERV NET, Mobility management, service discovery, disconnected operation, Dynamic configuration, auto registration, content based routing, Backbone Technology: Electrical Backbone Networks – Optical Backbone Networks – Wireless Backbone Networks – Wireless Access Technology - Pervasive Web Application architecture- Access from PCs and PDAs - Access via WAP.

UNIT III PERVASIVE DEVICES (9 Hrs)

Introduction with Case study of - PDA - Mobile Phone: Elements – Mobile Information Architecture - Mobile Phone Design - Android Overview – The Stack – Android User Interface – Preferences, the File System, the Options Menu and Intents.

UNIT IV WIRELESS DEVICES AND SECURITY ISSUES IN MOBILE COMPUTING (9 Hrs)

Mobile phones-PDA-Design constraints in applications for handheld devices - Convergence Technologies- Call Routing-Voice over IP applications-IMS-Mobile VoIP. Security in mobile computing- Issues- Security Protocols-models-Security framework for mobile environment.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Case study on Emerging Wireless Technologies, IEEE 802.20 Mobile Broadband Wireless Access.

Text Books

1. Debashissaha, Amitava Mukherjee," Networking Infrastructure for Pervasive Computing, Springer International edition, 2011.
2. Asoke K Talukder and Roopa R Yavagal, "Mobile Computing", Tata Mc Grawhill, 2010.
3. Natalia Olifer and Victor Olifer," Computer Networks principles. technologies and protocols for network design", Wiley, 2015

Reference Books

1. Frank Adelstein, Sandeep K S Gupta, Golden G Richard III, Loren Schwiebert, Fundamentals of mobile and pervasive computing, TMH, 2007.
2. Jochen Burkhardt, Horst Henn, Stefan Hepper, Klaus Rindtorff and Thomas Schack, "Pervasive Computing: Technology and Architecture of Mobile Internet Applications," Addison-Wesley, ISBN:0201722151,2002.
3. Uwe Hansmann, L.Merk, M.Nicklous, T.Stober and U.Hansmann, Pervasive computing (Springer Professional Computing),'' Springer Verlag, ISBN: 3540002189,2003.
4. Mullet,"Introduction to wireless telecommunications systems and networks", cengage learning, 2010.

5. Holger Karl,Andreas Willig,"Protocols & Architectures for WSN",John Wiley,2012

Web Resources

1. https://en.wikipedia.org/wiki/Ubiquitous_computing
2. http://www.nptel.iitm.ac.in/courses
3. https://www.isoc.org
4. https://www.ijarcce.com/upload/2015/december-15/IJARCCE%203.pdf
5. https://internetofthingsagenda.techtarget.com/definition/pervasive-computing-ubiquitous-computing

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	-	1
CO2	2	-	3	3	1	1	3	-	1
CO3	2	-	3	3	1	1	3	-	1
CO4	2	-	3	3	1	1	3	-	1
CO5	2	2	3	3	2	1	3	-	1

P20VEE327	ROBOTICS AND AUTOMATION	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To learn various robot structures and their workspace
- To develop student's skills in perform kinematics analysis of robot systems
- To provide the student with some knowledge and analysis skills associated with trajectory planning
- To learn the concepts of robot control techniques and its applications
- To study the robotic systems using processor models

Course Outcomes

After completion of the course, the students are able to

CO1 - Explain the fundamentals of robotics and its components. **(K2)**

CO2 - Ability to apply spatial transformation to obtain forward kinematics equation of robot manipulators. **(K3)**

CO3 - Demonstrate an ability to generate joint trajectory for motion planning. **(K3)**

CO4 - Understand the application of Robots and its operations. **(K2)**

CO5 - Develop simple robot control systems integrating perception, planning, and action. **(K4)**

UNIT I INTRODUCTION (9 Hrs)

Definition-Classification-History - Robots Components-Degrees of freedom-Robot joints- coordinates - Reference frames-workspace **-** actuators-sensors- Position, velocity and acceleration sensors-Torque sensors-tactile and touch sensors-proximity and range sensors- vision system-social issues.

UNIT II ROBOT ARM KINEMATICS (9 Hrs)

Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation – Denavit Hattenberg representation and various arm configurations.

UNIT III ROBOT ARM DYNAMICS (9 Hrs)

Lagrange - Euler formulation, joint velocities - kinetic energy - potential energy and motion equations – generalized D'Alembert equations of motion.

UNIT IV ROBOT APPLICATIONS (9 Hrs)

Material Transfer & Machine Loading / Unloading - General Consideration in robot material handling transfer applications – Machine loading and unloading.

Processing Operations: Spot welding – Continuous arc welding - spray coating – other processing operations using robots.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Design and develop robotic arm using ARM processor, Line follower models.

Text Books

1. R.K. Mittal and I J Nagrath, "Robotics and Control", Tata Mac Graw Hill, Fourth Reprint 2003.
2. Saeed B. Niku,"Introduction to Robotics ", Pearson Education, 2002.
3. Mikell P Groover, Nicholas G Odrey, Mitchel Weiss, Roger N Nagel, Ashish Dutta, "Industrial Robotics, Technology programming and Applications", McGraw Hill, 2012.

Reference Books

1. S.R. Deb, "Robotics Technology and flexible automation", Tata McGraw-Hill Education., 2009.
2. Richard D. Klafter, Thomas. A, ChriElewski, Michael Negin, "Robotics Engineering an Integrated Approach", PHI Learning., 2009.
3. Carl D. Crane and Joseph Duffy, "Kinematic Analysis of Robot manipulators", Cambridge University press, 2008.
4. Richard D Klafter, Thomas A Chmielewski, Michael Negin, "Robotics Engineering – An Integrated Approach", Eastern Economy Edition, Prentice Hall of India P Ltd., 2006.
5. Mikell P Groover, Nicholas G Odrey, Mitchel Weiss, Roger N Nagel, Ashish Dutta, "Industrial Robotics, Technology programming and Applications", McGraw Hill, 2009.

Web Resources

1. http:// www.nptel.iitm.ac.in
2. http://www.ocw.mit.edu
3. https://www.edx.org/learn/robotic-process-automation
4. https://www.iare.ac.in/sites/default/files/lecture_notes/ROBOTICS_LECURE_NOTES
5. https://lecturenotes.in/m/21711-note-of-automation-and-robotics-by-akash-sharma

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	-	3
CO2	2	-	3	3	1	1	3	-	3
CO3	2	-	3	3	1	1	3	-	3
CO4	2	-	3	3	1	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

P20VEE328	SYSTEM- ON-CHIP DESIGN	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To understand the components of system, hardware and software
- To know the basic concepts of processor architecture and instructions
- To describe external and internal memory of SOC
- To understand SOC customization and reconfiguration technologies
- To explain SOC design approach

Course Outcomes

After completion of the course, the students are able to

CO1 - Memorize the system architecture, components of system hardware and software. **(K2)**

CO2 – Explain the basic concepts of processor architecture and instructions and delays. **(K2)**

CO3 - Describe external and internal memory of SOC and organization. **(K3)**

CO4 – Explain SOC customization and reconfiguration technologies. **(K2)**

CO5 - Apply the knowledge of SOC design in real time applications. **(K3)**

UNIT I INTRODUCTION (9 Hrs)

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, an approach for SOC Design, System Architecture and Complexity.

UNIT II PROCESSORS (9 Hrs)

Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III MEMORY DESIGN FOR SOC (9 Hrs)

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction**.**

UNIT IV INTERCONNECT CUSTOMIZATION AND CONFIGURATION (9 Hrs)

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration -overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

SOC Design approach: simulate and verify AES algorithms, design and evaluation of Image compression JPEG compression.

Text Books

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd. 2012.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., Addison Wesley Professional 2000.
3. D. C. Black, J. Donovan, B. Bunton, A. Keist, SystemC: From the Ground Up, Second Edition, Springer, 2010.

Reference Books

1. Ricardo Reis," Design of System on a Chip: Devices and Components" 1st Ed., Springer. 2004,
2. Jason Andrews**, "**Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) Jason Andrews, Newnes, 2004.
3. Prakash Rashinkar, Peter Paterson and Leena Singh L, "System on Chip Verification – Methodologies and Techniques, Kluwer Academic Publishers, 2001.
4. P. Marwedel, Embedded System Design: Embedded Systems Foundations of Cyber-Physical Systems, Third Edition, Springer, 2018.

5. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling, Synthesis, Verification, Springer, 2009.

Web Resources

1. http://ic.sjtu.edu
2. http://nptel.iitm.ac.in
3. https://www.coursera.org/lecture/fpga-intro/programmable-system-on-chip-X5Gaq
4. https://ieeexplore.ieee.org/document/5490602
5. https://www.electronics-tutorial.net/System-On-Chip/SOC-Designs/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	3	-
CO2	2	-	3	3	1	1	3	3	-
CO3	2	-	3	3	1	1	3	3	-
CO4	2	-	3	3	1	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VEE329	VLSI FOR WIRELESS COMMUNICATION	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To study the design concepts of low noise amplifiers
- To understand the various types of mixers designed for wireless communication.
- To describe and design PLL and VCO.
- To understand the concepts of CDMA in wireless communication
- To design Mixer circuits and Frequency Synthesizers

Course Outcomes

After completion of the course, the students will be able to

CO1 - Describe the components and devices required for transmission **(K2)**
CO2 - Demonstrate the various mixer circuits **(K3)**
CO3 - Interpret the concept of frequency synthesizers **(K3)**
CO4 - Explain the concepts of sub systems **(K2)**
CO5 - Simulate VLSI circuits required for wireless communication **(K4)**

UNIT I COMPONENTS AND DEVICES (9 Hrs)

Integrated inductors, resistors, MOSFET and BJT Amplifier Design: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers

UNIT II MIXERS (9 Hrs)

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion – Switching Mixer - Distortion in Unbalanced Switching Mixer – Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer

UNIT III FREQUENCY SYNTHESIZERS (9 Hrs)

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).

UNIT IVSUB SYSTEMS (9 Hrs)

Data converters in communications, Design of adaptive Filters, equalizers and transceivers.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Simulation for different Mixer circuits and Frequency Synthesizers using the appropriate simulation tool.

Text Books

1. Thomas H.Lee, “The Design of CMOS Radio –Frequency Integrated Circuits’, Cambridge University Press ,2003.
2. Bosco H Leung “VLSI for Wireless Communication”, Pearson Education, 2014
3. Emad N. Farag and Mohamed I. Elmasry “Mixed Signal VLSI Wireless Design: Circuits and Systems”, Springer, 2013

Reference Books

1. BehzadRazavi, “Design of Analog CMOS Integrated Circuits” McGraw-Hill, 2016.
2. B.Razavi ,”RF Microelectronics” , Prentice-Hall ,2011
3. Thamarai Selvan and N. Pasupathy,” Wireless Network System in VLSI System Design: Secured Routing Protocol Technique”, LAP Lambert Academic Publishing,2020
4. Dutta, D., Kar, H., Kumar, C.and Bhadauria, V,” Advances in VLSI, Communication, and Signal Processing” Springer, 2018.

5. Ke-Lin Du and M. N. S. Swamy," Wireless Communication Systems: From RF Subsystems to 4G Enabling Technologies", Cambridge University Press,2019

Web References

1. https://nptel.ac.in/courses/106/106/106106167/
2. www.aticourses.com/Advanced%20Topics%20in%20Digital%20Signals
3. www.nptelvideos.in/2012/12/wireless-communication.html
4. www.springer.com/us/book/9781461409854/
5. https://nptel.ac.in/courses/117/102/117102062/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	3	-
CO2	2	-	3	3	1	1	3	3	-
CO3	2	-	3	3	1	1	3	3	-
CO4	2	-	3	3	1	1	3	3	-
CO5	2	2	3	3	2	1	3	3	-

P20VEE330	RISC PROCESSOR ARCHITECTURE AND PROGRAMMING	L	T	P	C	Hrs
		3	-	-	3	45

Course Objectives

- To introduce students with the architecture and operation of AVR microcontrollers
- To familiarize the students with interfacing of AVR microcontrollers
- To understand the architecture and programming of ARM processors
- To gain knowledge on development of ARM applications
- To provide strong foundation for designing real world applications using ARM processors

Course Outcomes

After completion of the course, the students are able to

CO1 - Explain the internal architecture and organization of AVR microcontroller. **(K2)**

CO2 - Design the interfacing for AVR microcontroller. **(K3)**

CO3 - Analyze the internal architecture of ARM Processors. **(K4)**

CO4 - Describe the exception, interrupts and interrupt handling schemes. **(K3)**

CO5 - Design and implement ARM processor systems. **(K2)**

UNIT I AVR MICROCONTROLLER ARCHITECTURE (9 Hrs)

Architecture – memory organization – Addressing modes – Instruction set – Programming Techniques – Assembly language & C programming- Development Tools – Cross Compilers – Hardware Design Issues.

UNIT II PERIPHERAL OF AVR MICROCONTROLLER (9 Hrs)

I/O Memory – EEPROM – I/O Ports –SRAM –Timer –UART – Interrupt Structure- Serial Communication with PC – ADC/DAC Interfacing.

UNIT III ARM ARCHITECTURE AND PROGRAMMING (9 Hrs)

Arcon RISC Machine – Architectural Inheritance – Core & Architectures - Registers – Pipeline - Interrupts – ARM organization - ARM processor family – Co-processors. Instruction set – Thumb instruction set – Instruction cycle timings - ARM Programmer's model – ARM Development tools – ARM Assembly Language Programming and 'C' compiler programming.

UNIT IV ARM APPLICATION DEVELOPMENT (9 Hrs)

Introduction to DSP on ARM –FIR Filter – IIR Filter – Discrete Fourier transform – Exception Handling – Interrupts – Interrupt handling schemes- Firmware and boot loader – Example: Standalone - Embedded Operating Systems – Fundamental Components - Example Simple little Operating System.

UNIT V INSTRUCTIONAL ACTIVITY (9 Hrs)

Interfacing of various I/O devices and memory with ARM processor for home automation.

Text Books

1. Steve Furber, ARM system on chip architecture, 2nd Edition, Addision Wesley longman, 2011.
2. Mitesh Limachia and Nikhil Kothari, "Modeling and Simulation of Arm Processor Architecture", LAP Lambert Academic Publishing, 2012
3. Sarmad Naimi, Muhammad Ali Mazidi, and Sepehr Naimi, "The AVR Microcontroller and Embedded Systems Using Assembly and C: Using Arduino Uno and Atmel Studio", Microdigitaled, 2017

Reference Books

1. Andrew N. Sloss, Dominic Symes, Chris Wright, John Rayfield, *ARM System.* Developer's Guide Designing and Optimizing System Software, Elsevier Science, 2016.
2. Trevor Martin, The Insider's Guide to The Philips ARM7-Based Microcontrollers, An Engineer's Introduction to The LPC2100 Series, Hitex (UK) Ltd., 2005. Dananjay V. Gadre, Programming and Customizing the AVR microcontroller, McGraw Hill, 2001.
3. Lyla B Das, The X86 Microprocessors: Architecture and Programming, Pearson Education India, 2010.
4. Sivarama P. Dandamudi, Guide to RISC Processors, Springer, 2005.
5. Bisht Santul, "Arm Processor - A New Era in Low Power Application", LAP Lambert Academic Publishing, 2012

Web Resources

1. http://www.avr.com.
2. http://www.arm.com.

3. https://nptel.ac.in/courses/117/106/117106111/
4. https://nptel.ac.in/courses/106/105/106105193/
5. https://developer.arm.com/tools-and-software/simulation-models

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
CO1	2	-	3	3	1	1	3	-	3
CO2	2	-	3	3	1	1	3	-	3
CO3	2	-	3	3	1	1	3	-	3
CO4	2	-	3	3	1	1	3	-	3
CO5	2	2	3	3	2	1	3	-	3

AUDIT COURSES

Sl. No.	Course Code	Course Title
1	P20ACTX01	English for Research Paper Writing
2	P20ACTX02	Disaster Management
3	P20ACTX03	Sanskrit for Technical Knowledge
4	P20ACTX04	Value Education
5	P20ACTX05	Constitution of India
6	P20ACTX06	Pedagogy Studies
7	P20ACTX07	Stress Management by Yoga
8	P20ACTX08	Personality Development Through Life Enlightenment Skills
9	P20ACTX09	Unnat Bharat Abhiyan

P20ACTX01	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C	Hrs
		2	-	-	-	30

Course Objectives

- Teach improve writing skills and level of readability.
- Tell about what to write in each section.
- Summarize the skills needed when writing a Title.
- Infer the skills needed when writing the Conclusion.
- Ensure the quality of paper at very first-time submission.

Course Outcomes

CO1- Understand that how to improve your writing skills and level of readability.
CO2- Learn about what to write in each section.
CO3- Understand the skills needed when writing a Title.
CO4- Understand the skills needed when writing the Conclusion.
CO5- Ensure the good quality of paper at very first-time submission.

UNIT I INTRODUCTION TO RESEARCH PAPER WRITING (06 Hrs)

Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

UNIT II PRESENTATION SKILLS (06 Hrs)

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction.

UNIT III TITLE WRITING SKILLS (06 Hrs)

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT IV RESULT WRITING SKILLS (06 Hrs)

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions.

UNIT V VERIFICATION SKILLS (06 Hrs)

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission

References

1. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press, 2006.
3. Goldbort R Writing for Science, Yale University Press (available on Google Books), 2006.
4. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book, 1998.

P20ACTX02 **DISASTER MANAGEMENT**

L	T	P	C	Hrs
2	-	-	-	30

Course Objectives

- Summarize basics of disaster explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches.

Course Outcomes

CO1 - Ability to summarize basics of disaster.
CO2 - Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
CO3 - Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
CO4 - Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
CO5- Ability to develop the strengths and weaknesses of disaster management approaches.

UNIT I INTRODUCTION (06 Hrs)

Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II REPERCUSSIONS OF DISASTERS AND HAZARDS (06 Hrs)

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT III DISASTER PRONE AREAS IN INDIA (06 Hrs)

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post-Disaster Diseases and Epidemics.

UNIT IV DISASTER PREPAREDNESS AND MANAGEMENT (06 Hrs)

Preparedness: Monitoring of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V RISK ASSESSMENT (06 Hrs)

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival

Reference Books

1. Goel S. L., Disaster Administration And Management Text And Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2. NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies 'New Royal book Company,2007.
3. Sahni, Pardeep Et.Al., "Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi,2001.

P20ACTX03	SANSKRIT FOR TECNICAL KNOWLEDGE	L	T	P	C	Hrs
		2	-	-	-	30

Course Objectives

- Illustrate the basic Sanskrit language
- Recognize Sanskrit, the scientific language in the world
- Appraise learning of Sanskrit to improve brain functioning
- Relate Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
- Extract huge knowledge from ancient literature

Course Outcomes

CO1- Understanding basic Sanskrit language.
CO2- Write sentences.
CO3- Know the order and roots of Sanskrit.
CO4- Know about technical information about Sanskrit literature.
CO5- Understand the technical concepts of Engineering.

UNIT I ALPHABETS **(06 Hrs)**
Alphabets in Sanskrit.

UNIT II TENSES AND SENTENCES **(06 Hrs)**
Past/Present/Future Tense - Simple Sentences.

UNIT III ORDER AND ROOTS **(06 Hrs)**
Order - Introduction of roots of Engineering-Electrical, Mechanical, Architecture, Mathematics.

UNIT IV SANSKRIT LITERATURE **(06 Hrs)**
Technical information about Sanskrit Literature.

UNIT V TECHNICAL CONCEPTS OF ENGINEERING **(06 Hrs)**
Technical concepts.

Reference Books

1. "Abhyaspustakam" – Dr. Vishwas, Samskrita-Bharti Publication, New Delhi.
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication.
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi, 2017.

P20ACTX04	VALUE EDUCATION	L	T	P	C	Hrs
		2	-	-	-	30

Course Objectives

- Understand value of education and self-development
- Imbibe good values in students
- Let they should know about the importance of character

Course Outcomes

Students will be able to

- Knowledge of self-development.
- Learn the importance of Human values.
- Developing the overall personality.

UNIT I

Values and self-development–Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non-moral valuation. Standards and principles. Value judgements of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively.

UNIT II

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline

UNIT III

Personality and Behavior Development-Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brother hood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature.

UNIT IV

Character and Competence–Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role.

Reference Books

1. Chakroborty, S.K.“Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi.

P20ACTX05 **CONSTITUTION OF INDIA**

L	T	P	C	Hrs
2	-	-	-	30

Course Objectives

- Understand the premises informing the twin themes of liberty and freedom from a civil rights Perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional.
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.

Course Outcomes

Students will be able to

CO1 - Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.

CO2 - Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.

CO3 - Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections.

CO4 - Discuss the passage of the Hindu Code Bill of 1956.

UNIT I HISTORY OF MAKING OF THE INDIAN CONSTITUTION (05 Hrs)

History, Drafting Committee, (Composition & Working).

UNIT II PHILOSOPHY OF THE INDIAN CONSTITUTION (05 Hrs)

Preamble, Salient Features.

UNIT III CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES (05 Hrs)

Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT IV ORGANS OF GOVERNANCE (05 Hrs)

Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V LOCAL ADMINISTRATION (05 Hrs)

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT VI ELECTION COMMISSION (05 Hrs)

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

Reference Books

1. "The Constitution of India,1950(Bare Act), Government Publication.
2. Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,1st Edition, 2015.
3. M.P. Jain, Indian Constitution Law, 7th Edition, Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015 "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi, 2017.

P20ACTX06 **PEDAGOGY STUDIES**

L	T	P	C	Hrs
2	-	-	-	30

Course Objectives

- Review existing evidence on their view topic to inform programme design and policy.
- Making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes

Students will be able to understand:

- What pedagogical practices are being used by teachers informal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

UNIT I INTRODUCTION AND METHODOLOGY: **(06 Hrs)**

Aims and rationale, Policy background, Conceptual framework and terminology - Theories of learning, Curriculum, Teacher education - Conceptual framework, Research questions – Overview of methodology and Searching.

UNIT II THEMATIC OVERVIEW **(06 Hrs)**

Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries - Curriculum, Teacher education.

UNIT III EVIDENCE ON THE EFFECTIVENESS OF PEDAGOGICAL PRACTICES **(06 Hrs)**

Methodology for the in-depth stage: quality assessment of included studies - How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? - Theory of change - Strength and nature of the body of evidence for effective pedagogical practices - Pedagogic theory and pedagogical approaches - Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT IV PROFESSIONAL DEVELOPMENT **(06 Hrs)**

Professional development: alignment with classroom practices and follows up support – Peer support - Support from the head teacher and the community - Curriculum and assessment - Barriers to learning limited resources and large class sizes.

UNIT V RESEARCH GAPS AND FUTURE DIRECTIONS **(06 Hrs)**

Research design – Contexts – Pedagogy - Teacher education - Curriculum and assessment - Dissemination and research impact.

Reference Books

1. Ackers J, HardmanF (2001) Classroom interaction in Kenyan primary schools, Compare, 31(2): 245- 261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36(3):361-379.
3. Akyeampong K (2003) Teacher training in Ghana-does it count? Multi-site teacher education research project (MUSTER) country report 1. London:DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33(3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.

P20ACTX07 **STRESS MANAGEMENT BY YOGA**

L	T	P	C	Hrs
2	-	-	-	30

Course Objectives

- To achieve overall health of body and mind.
- To overcome stress.

Course Outcomes

Students will be able to:

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency.

UNIT I

Definitions of Eight parts of yoga. (Ashtanga).

UNIT II

Yam and Niyam - Do`s and Don't's in life - i) Ahinsa, satya, astheya, bramhacharya and aparigraha, ii) Ahinsa, satya, astheya, bramhacharya and aparigraha.

UNIT III

Asan and Pranayam - Various yog poses and their benefits for mind & body - Regularization of breathing techniques and its effects-Types of pranayam.

Reference Books

1. 'Yogic Asanas for Group Tarining-Part-I":Janardan Swami Yoga bhyasi Mandal, Nagpur.
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata.

P20ACTX08	PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS	L	T	P	C	Hrs
		2	-	-	-	30

Course Objectives

- To learn to achieve the highest goal happily.
- To become a person with stable mind, pleasing personality and determination.
- To awaken wisdom in students.

Course Outcomes

Students will be able to

CO1 - Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life.

CO2 - The person who has studied Geeta will lead the nation and mankind to peace and prosperity.

CO3 - Study of Neet is hatakam will help in developing versatile personality of students.

UNIT I

Neetisatakam-holistic development of personality - Verses- 19,20,21,22 (wisdom) - Verses- 29,31,32 (pride & heroism) – Verses- 26,28,63,65 (virtue) - Verses- 52,53,59 (dont's) - Verses- 71,73,75,78 (do's) 4-Verses 18, 38,39 Chapter18 – Verses37,38,63.

UNIT II

Approach to day to day work and duties - Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48 - Chapter 3-Verses 13, 21, 27, 35 Chapter 6-Verses 5,13,17,23, 35 - Chapter 18-Verses 45, 46, 48.model – shrimad bhagwad geeta - Chapter2- Verses 17, Chapter 3-Verses 36,37,42 – Chapter.

UNIT III

Statements of basic knowledge – Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 Chapter12 -Verses 13, 14, 15, 16,17, 18 - Personality of role.

Reference Books

1. Gopinath, Rashtriya Sanskrit Sansthanam P, Bhartrihari's Three Satakam, Niti-sringar- vairagya, New Delhi,2010.
2. Swami Swarupananda, Srimad Bhagavad Gita, Advaita Ashram, Publication Department, Kolkata, 2016.