SRI MANAKULA VINAYAGAR
ENGINEERING COLLEGE
(An Autonomous Institution)
Puducherry

25 years of ACADEMIC EXCELLENCE

Sixth BoS Meeting

July 21, 2023 (Friday)
Seminar Hall,
Department of Electronics and Communication Engineering

- **M.Tech – Electronics and Communication Engineering**
- **M.Tech – VLSI and Embedded Systems**
- **Ph.D – Electronics and Communication Engineering**

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SRI MANAKULA VINAYAGAR ENGINEERING COLLEGE

(An Autonomous Institution)

Puducherry - 605 107

6th PG - Board of Studies Meeting in the department of
Electronics and Communication Engineering

for the Programme
M.Tech – Electronics and Communication Engineering
M.Tech – VLSI and Embedded Systems
Ph.D – Electronics and Communication Engineering

Venue
Seminar Hall, Department of ECE
Sri Manakula Vinayagar Engineering College
Madagadipet, Puducherry – 605 107

Date & Time

21-07-2023 & 11.30 am

BOARD OF STUDIES MEETING

The Sixth Board of Studies meeting for PG and Research programs was held on July 21, 2023 at 11:30 AM in the Seminar Hall, Department of ECE, Sri Manakula Vinayagar Engineering College.

BoS Members

Sl. No	Name of the Member	Designation
1	**Dr. P. Raja** Professor and Head, Department of ECE	Chairman
2	**Dr. Gerardine Immaculate Mary** Professor, Department of Embedded Systems, Vellore Institute of Technology (VIT), Vellore, Tamil Nadu, India	Expert Member (University Nominee)
3	**Dr. N. Venkateswaran** Professor, Department of ECE, SSN - College of Engineering, Kalavakkam, Tamil Nadu, India	Expert Member (Academic Council Nominee)
4	**Dr. V. R. Vijayakumar** Associate Professor & Head, Department of ECE, Anna University, Regional Campus, Coimbatore	Expert Member (Academic Council Nominee)
5	**Mr. C. Gnanavel** General Manager, Production and Technology, Lenovo India Ltd., Puducherry	Industry Member
6	**Dr. V. Bharathi,** Professor / ECE **Specialization:** Wireless Communication	Member

7	**Dr. R. Ramya,** Professor/ ECE **Specialization:** ECE	Member
8	**Dr. R. Kurinjimalar,** Professor / ECE **Specialization:** Mobile Satellite Communication	Member
9	**Dr. J. Pradeep, Associate** Professor / ECE **Specialization:** Image Processing	Member
10	**Prof. R. Ilaiyaraja,** Assistant Professor / ECE **Specialization:** VLSI Design	Member
11	**Dr. T. Gayathri,** Professor **Specialization:** Mathematics	Member
12	**Prof. K. Oudayakumar,** Associate Professor **Specialization:** Physics	Member
13	**Dr. S. Savithri,** Professor **Specialization:** Chemistry	Member
14	**Dr.D. Jaichithra,** Associate Professor **Specialization:** English	Member
15	**Mr. G. Dharanidharan** Birlasoft Limited, Old Mahabalipuram Road, Chennai – 600096	Alumni Member

AGENDA OF THE MEETING

BoS /2023/PG/ECE 6.1

To review and confirm the minutes of fifth BoS meeting held on 17th September 2023

BoS /2023/PG/ECE 6.2

To discuss and approve Regulations 2023 (R-2023) for the M.Tech., Programmes for the students admitted from the academic year 2023-24

- M.Tech – Electronics and Communication Engineering
- M.Tech – VLSI and Embedded Systems

BoS /2023/PG/ECE 6.3

To discuss and approve curriculum structure and Syllabi for Semester I and II for M.Tech Electronics and Communication Engineering Programme under the Regulations R-2023

BoS /2023/PG/ECE 6.4

To discuss and approve curriculum structure and Syllabi for Semester I and II for M.Tech VLSI and Embedded Systems Programme under the Regulations R-2023

BoS /2023/PG/ECE 6.5

To appraise and approve the professional electives and employability enhancement courses chosen by the students under Regulations 2020

BoS /2023/PG/ECE 6.6

To discuss about the Internship course for PG programmes from the Academic Year 2021-22 onwards

BoS /2023/PG/ECE 6.7

To appraise and approve the list of eligible students called for personal interview for PhD programme in Electronics and Communication Engineering

BoS /2023/PG/ECE 6.8

Any other item with the permission of chair

MINUTES OF THE MEETING

Dr. P. Raja, Chairman of the Board of Studies (BoS), opened the Sixth BoS meeting for the M.Tech., and Research programs. He then proceeded to discuss the agenda items.

BoS / 2023 / PG/ ECE 6.1

To review and confirm the fifth BoS meeting minutes held on 17th September 2022

The fifth Board of Studies (BoS) meeting for M.Tech. in Electronics and Communication Engineering and M.Tech. in VLSI and Embedded Systems under Regulations 2020 was held on September 17, 2022. The minutes of the meeting were reviewed and confirmed.

Approved and Confirmed

BoS / 2023 / PG/ ECE 6.2

To discuss and approve Regulations 2023 (R-2023) for the M.Tech., Programmes for the students admitted from the academic year 2023-24

- **M.Tech – Electronics and Communication Engineering**
- **M.Tech – VLSI and Embedded Systems**

Members discussed the Regulations 2023 (R-2023) for the following M.Tech.. programs for students admitted from the academic year 2023-2024:

- M.Tech. in Electronics and Communication Engineering
- M.Tech. in VLSI and Embedded Systems

Approved and Recommended to the Academic Council

BoS / 2023 / PG/ ECE 6.3

To discuss and approve curriculum structure and Syllabi for Semester I and II for M.Tech., Electronics and Communication Engineering Programme under the Regulations R-2023

- In semester I, a High-Speed Electronics theory course has been introduced, with the suggestion from members to update the course content based on modern electronic devices.
- Semester II brought the introduction of a course on “Embedded Processors”, with members proposing the inclusion of recent high-speed embedded processors in the syllabus.
- Additionally, members have recommended changing the course title of "Millimeter Wave Communication Networks" to "High-Frequency Communication System" in Semester II, with a syllabus containing 3 units of Millimeter wave communication and 2 units of optical communication.
- Members have expressed their appreciation for the Employability Enhancement Courses and Audit Courses offered in both semesters I and II under Regulations 2023.
- Members have discussed the professional elective course offered in both semesters I and II, as per Regulation 2023.

Approved with minor corrections and Recommended to the Academic Council

All the suggestions are considered and updated in the respective courses. The details are given in

Annexure – I (A): Curriculum of M. Tech – Electronics and Communication Engineering
Annexure–I (B): Updated Syllabus M. Tech – Electronics and Communication Engineering

BoS / 2023 / PG/ ECE 6.4

To discuss and approve curriculum structure and Syllabi for Semester I and II for M.Tech VLSI and Embedded Systems Programme under the Regulations R-2023

- Members have suggested changing the course title to “Electronic Design Automation Tools” instead of “Digital System Design” course to provide an advanced level of learning in semester-I. They also suggested including recent automation tools in the syllabus to get more exposure at the industry level.
- The members suggested replacing the embedded networking course with the “Embedded Processors” course in semester 2 to provide knowledge on developing IoT models by utilizing these processors.
- The members appreciated the Employability Enhancement Courses and Audit Courses offered in Regulations 2023.
- Members have discussed the professional elective course offered in semesters 1 and 2 as per Regulation 2023.

Approved with minor corrections and Recommended to the Academic Council

All the suggestions are considered and updated in the respective courses. The details are given in

Annexure – II (A): Curriculum of M. Tech – VLSI and Embedded Systems
Annexure–II (B): Updated Syllabus M. Tech – VLSI and Embedded Systems

BoS / 2023 / PG/ ECE 6.5

To appraise and approve the professional electives and employability enhancement courses chosen by the students under Regulations 2020

List of professional elective courses by the students from M.Tech - VLSI & ES

Semester	Course Code	Course Title
II	P20VEE210	Internet of Things
II	P20VEE212	Industrial Automation using PLC and SCADA

Noted and Approved

BoS / 2023 / PG/ ECE 6.6

To ratify the Internship course for PG programmes from the Academic Year 2021-22 onwards

The students from the M.Tech - ECE programme have completed the Internship

Enroll No.	Register No	Name of the Student	Company Name	Duration
211727	21PEC001	Divyadharshini P	Qmax Systems India Pvt. Ltd	1 months
210703	21PEC003	Nithya Valli.P	Qmax Systems India Pvt. Ltd	1 months

The students from the M.Tech- VLSI programme have completed the Internship

Enroll No.	Register No	Name of the Student	Company Name	Duration
210962	21PVE001	Balaji M	Idea Lab, SMVEC	1 months
210864	21PVE002	Nigithadharshini S	Qmax Systems India Pvt. Ltd	1 months
210797	21PVE003	Priyadharshni R	Idea Lab, SMVEC	1 months
211072	21PVE004	Sivaram Kumar R	Idea Lab, SMVEC	1 months
211062	21PVE005	Sivaraman S	Idea Lab, SMVEC	1 months

- Members esteemed the progress of the PG Internship.

Noted and Approved

BoS / 2023 / PG/ ECE 6.7

To appraise and approve the list of eligible students called for personal interview for PhD programme in Electronics and Communication Engineering

During the academic year 2022-2023, the Ph.D admission process was discussed by a member. In total, 70 candidates applied for the Ph.D programme, with 11 submitting applications specifically for Electronics and Communication Engineering. Out of those 11 candidates, 7 successfully passed the entrance examination and have been invited for a personal interview

List of eligible candidates called for personal interview

S. No	Name of the Candidate
1	D. Mary Getsy
2	R. Gayathri
3	J. Suganya
4	P. Srividdhya
5	B. Menaga
6	V. M. Navaneetha Krishnan
7	V. Logisvary

Approved and Recommended

BoS / 2023 / PG/ ECE 6.8

Any other item with the permission of chair

The syllabus is well-structured and covers advanced future technology topics. Additionally, the members encourage research scholars to publish their papers in reputable journals.

Dr. P. Raja, Chairman – BoS and Head of Department, Electronics and Communication Engineering, concluded the meeting at 12.30 pm with vote of thanks.

Dr. P. RAJA
Board Chairman - ECE

Dr. GERARDINE IMMACULATE MARY
Professor, Department of Embedded Systems,
Vellore Institute of Technology (VIT), Vellore
(Expert Member - University Nominee)

Dr. N. VENKATESWARAN
Professor, Department of ECE,
SSN College of Engineering, Kalavakkam
(Expert Member – AC Nominee)

Dr. V. R. VIJAYAKUMAR
Associate Professor & Head, Department of ECE,
Anna University, Regional Campus, Coimbatore
(Expert Member – AC Nominee)

Mr. C. GNANAVEL
Manager, Production and Technology,
Lenovo India Ltd., Puducherry
(Industry. Member)

Mr. DHARANIDHARAN. G
Associated Functional Consultant,
Birlasoft Limited, Chennai
(Alumni Member)

Dr. R. RAMYA
Professor/ ECE
(Member)

Dr. V. BHARATHI
Professor / ECE
(Member)

Dr. R. KURINJIMALAR
Associate Professor / ECE
(Member)

Dr. J. PRADEEP
Associate Professor / ECE
(Member)

Prof. R. ILAIYARAJA,
Assistant Professor / ECE
(Member)

Dr.T.GAYATHRI
Professor / Mathematics
(Member)

Prof. K. OUDAYAKUMAR
Associate Professor / Physics
(Member)

Dr.S.SAVITHIRI
Professor / Chemistry
(Member)

Dr. D. JAICHITHRA
Professor / English
(Member)

ANNEXURE – 1 (A): CURRICULUM

M.Tech – Electronics and Communication Engineering

SRI MANAKULA VINAYAGAR

ENGINEERING COLLEGE

(An Autonomous Institution)

Puducherry

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

M.TECH.

ELECTRONICS AND COMMUNICATION ENGINEERING

(REGULATIONS-2023)

CURRICULUM & SYLLABI

25 years of ACADEMIC EXCELLENCE

VISION AND MISSION OF THE INSTITUTE

VISION

To be globally recognized for excellence in quality education, innovation and research for the transformation of lives to serve the society.

MISSION

M1: Quality Education	To provide comprehensive academic system that amalgamates the cutting edge-technologies with best practices
M2: Research and Innovation	To foster value-based research and innovation in collaboration with industries and institutions globally for creating intellectuals with new avenues
M3: Employability and Entrepreneurship	To inculcate the employability and entrepreneurial skills through value and skill-based training
M4: Ethical Values	To instill deep sense of human values by blending societal righteousness with academic professionalism for the growth of society

VISION AND MISSION OF THE DEPARTMENT

VISION

Facilitate academic excellence and research among Electronics and Communication Engineers to meet the Global needs with high competence and ethical professionalism

MISSION

M1: Academic Excellence	To impart learning skills to meet the global challenges in the field of Electronics and Communication Engineering
M2: Research and Innovation	To provide excellence in research and innovation through multidisciplinary specialization
M3: Employability and Entrepreneurship	To enhance inter and intrapersonal skills among students to make them employable and entrepreneurs
M4: Ethics	To inculcate the significance of human values and professional skills to serve the society

PROGRAMME OUT COMES (POs)

PO1: Exploration of Research:
An ability to independently carry out research/investigation and development work to solve practical problems.

PO2: Technical Skill:

An ability to write and present a substantial technical report/document.

PO3: Expertise in Academics:

Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Scholarship of Knowledge:

Acquire in-depth knowledge of specific discipline or professional area, including wider and global perspective, with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge, and integration of the same for enhancement of knowledge.

PO5: Usage of Modern Tools:

Create, select, learn and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex engineering activities with an understanding of the limitations.

PO6: Ethical Practices and Social Responsibility:

Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Technical Knowledge

To develop intellectual combination of technology with modern electronics and communication systems through well-built technical acquaintance

PEO2: Leadership Skill

To endure changes and challenges in the areas of Electronics and Communication Engineering with good leadership skills.

PEO3: Research and Development

To identify the requisite of the nation, industry and come out with innovative solutions to maintain a sustainable position

PEO4: Professional Behavior

To promote competitive graduates global wise in Electronics and Communication Engineering

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Technical Knowledge in Electronics and Communication Engineering

Ability to understand the technological advancements in the field of electronics and communication by using modern design tools and sub system end processes

PSO2: Competency in Electronics

Apply research ideas to offer solutions for extant problems in areas including signal processing, image processing, consumer electronics, VLSI, Embedded with given requirements

PSO3: Competency in Communication

Ability to develop and provide optimal solutions to subsystems like RF, baseband of modern communication systems and networks.

SEMESTER–I

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23MAT101	Probability and Stochastic Process	BS	2	2	0	3	40	60	100
2	P23ECT101	Advanced Digital Communication	PC	3	0	0	3	40	60	100
3	P23ECT102	Millimeter Wave Communication Networks	PC	3	0	0	3	40	60	100
4	P23ECT103	High Speed Electronics	PC	3	0	0	3	40	60	100
5	P23HSTC01	Research Methodology and IPR	HS	2	0	0	2	40	60	100
6	P23ECE1XX	Professional Elective - I	PE	3	0	0	3	40	60	100
Practical										
7	P23ECP101	Advanced Digital Communication Laboratory	PC	0	0	4	2	50	50	100
8	P23HSPC101	Technical Report Writing & Seminar	HS	0	0	4	2	100	0	100
Ability Enhancement Course										
9	P23ECC1XX	Certification Course – I	AEC	0	0	4	-	100	-	100
10	P23ACT10X	Audit Course - I	AEC	2	0	0	-	100	-	100
							21	**590**	**410**	**1000**

SEMESTER–II

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23VETC01	Advanced Digital System Design	PC	3	0	0	3	40	60	100
2	P23VETC02	Embedded Processors	PC	3	0	0	3	40	60	100
3	P23VETC03	Embedded System Design	PC	3	0	0	3	40	60	100
4	P23ECT204	Digital Image and Video Processing	PC	3	0	0	3	40	60	100
5	P23ECE2XX	Professional Elective - II	PE	3	0	0	3	40	60	100
6	P23ECEXX	Professional Elective - III	PE	3	0	0	3	40	60	100
Practical										
7	P23ECP202	Digital Image and Video Processing laboratory	PC	0	0	4	2	50	50	100
8	P23HSPC202	Seminar on ICT-a hands on approach	HS	0	0	4	2	100	0	100
Ability Enhancement Course										
10	P23ECC2XX	Certification Course – II	AEC	0	0	4	-	100	-	100
11	P23ACT20X	Audit Course-II	AEC	2	0	0	-	100	-	100
Total							**22**	**590**	**410**	**1000**

SEMESTER–III

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23ECE3XX	Professional Elective - IV	PE	3	0	0	3	40	60	100
2	P23ECE3XX	Professional Elective - V	PE	3	0	0	3	40	60	100
3	P23ECE3XX	Professional Elective - VI	PE	3	0	0	3	40	60	100
Project Work										
4	P23ECW301	Project Phase - I	PA	0	0	12	6	50	50	100
5	P23ECW302	Internship	PA	0	0	0	2	100	-	100
Mandatory Course										
6	P23ECC301	NPTEL / GIAN / MOOC	AEC	0	0	0	-	100	-	100
Total							**17**	**370**	**230**	**600**

SEMESTER–IV

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Project Work										
1	P23ECW403	Project Phase - II	PA	0	0	24	12	50	50	100
Total							**12**	**50**	**50**	**100**

* Professional Elective Courses are to be selected from the list given in Annexure I

Ability Enhancement Courses are to be selected from the list given in Annexure II

** Audit Courses are to be selected from the list given in Annexure III

BS – Basic Science
HS – Humanity Science
PC – Professional Core
PE – Professional Elective
PA – Project Work
C – Common Course
AEC – Audit Course
AEC – Ability Enhancement Course

Credit Distribution

Semester- I	Semester - II	Semester - III	Semester - IV	Total
21	**22**	**17**	**12**	**72**

Total number of credits required to complete M.Tech in Electronics and Communication Engineering	**72 credits**

Annexure – A

PROFESSIONAL ELECTIVE COURSES

Professional Elective –I (Offered in Semester I)		
Sl. No.	**Course Code**	**Course Title**
1	P23ECE101	Advanced Microprocessor and Interfacing
2	P23ECE102	Image Processing and Recognition
3	P23ECE103	MIMO Systems
4	P23ECE104	Optical Communication and Networking
5	P23ECE105	Wireless Sensor Networks and its applications
Professional Elective – II (Offered in Semester II)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC01	Design of Analog and Mixed VLSI Circuits
2	P23VEEC02	Internet of Things and its Implementation
3	P23ECE206	Advanced Satellite Communication
4	P23ECE207	Mobile Communication System
5	P23ECE208	Statistical Information Processing
Professional Elective –III (Offered in Semester II)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC03	System on Chip Design
2	P23ECE309	Advanced Communication Network
3	P23ECE310	Advanced Radiation Systems
4	P23ECE311	Embedded Networking and Automation of Electrical System
5	P23ECE312	Industrial Electronics
Professional Elective–IV (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC04	Real Time Operating System
2	P23VEEC05	Cloud computing and Distributed System
3	P23ECE313	Automotive Embedded System
4	P23ECE314	Information and Network Security
5	P23ECE315	RF and Microwave Circuit Design
Professional Elective –V (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC06	Edge Computing
2	P23ECE316	Cognitive Radio Technology
3	P23ECE417	Embedded Computing
4	P23ECE418	Markov Chains and Queuing Systems
5	P23ECE419	Modeling and Simulation of Wireless Communication Systems
Professional Elective–VI (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23ECE420	Unmanned Aerial Vehicle
2	P23ECE421	Free Space Optical Networks
3	P23ECE422	Intelligent Control and Automation
4	P23ECE423	Multicarrier Wireless Communication
5	P23ECE424	Smart system design

Annexure – B

ABILITY ENHANCEMENT COURSES

S. No	Course Code	Course Title	Certified By
1	P23XXCX01	Adobe Photoshop	Adobe
2	P23XXCX02	Adobe Animate	Adobe
3	P23XXCX03	Adobe Dreamweaver	Adobe
4	P23XXCX04	Adobe After Effects	Adobe
5	P23XXCX05	Adobe Illustrator	Adobe
6	P23XXCX06	Adobe InDesign	Adobe
7	P23XXCX07	Autodesk AutoCAD -ACU	Autodesk
8	P23XXCX08	Autodesk Inventor - ACU	Autodesk
9	P23XXCX09	Autodesk Revit - ACU	Autodesk
10	P23XXCX10	Autodesk Fusion 360 - ACU	Autodesk
11	P23XXCX11	Autodesk 3ds Max - ACU	Autodesk
12	P23XXCX12	Autodesk Maya - ACU	Autodesk
13	P23XXCX13	Cloud Security Foundations	AWS
14	P23XXCX14	Cloud Computing Architecture	AWS
15	P23XXCX15	Cloud Foundation	AWS
16	P23XXCX16	Cloud Practitioner	AWS
17	P23XXCX17	Cloud Solution Architect	AWS
18	P23XXCX18	Data Engineering	AWS
19	P23XXCX19	Machine Learning Foundation	AWS
20	P23XXCX20	Robotic Process Automation / Medical Robotics	Blue Prism
21	P23XXCX21	Advance Programming Using C	CISCO
22	P23XXCX22	Advance Programming Using C ++	CISCO
23	P23XXCX23	C Programming	CISCO
24	P23XXCX24	C++ Programming	CISCO
25	P23XXCX25	CCNP Enterprise: Advanced Routing	CISCO
26	P23XXCX26	CCNP Enterprise: Core Networking	CISCO
27	P23XXCX27	Cisco Certified Network Associate - Level 2	CISCO
28	P23XXCX28	Cisco Certified Network Associate- Level 1	CISCO
29	P23XXCX29	Cisco Certified Network Associate- Level 3	CISCO
30	P23XXCX30	Fundamentals of Internet of Things	CISCO
31	P23XXCX31	Internet of Things / Solar and Smart Energy System with IoT	CISCO
32	P23XXCX32	Java Script Programming	CISCO
33	P23XXCX33	NGD Linux Essentials	CISCO
34	P23XXCX34	NGD Linux I	CISCO
35	P23XXCX35	NGD Linux II	CISCO
36	P23XXCX36	Advance Java Programming	Ethnotech
37	P23XXCX37	Android Programming / Android Medical App Development	Ethnotech
38	P23XXCX38	Angular JS	Ethnotech
39	P23XXCX39	Catia	Ethnotech
40	P23XXCX40	Communication Skills for Business	Ethnotech
41	P23XXCX41	Coral Draw	Ethnotech
42	P23XXCX42	Data Science Using R	Ethnotech
43	P23XXCX43	Digital Marketing	Ethnotech
44	P23XXCX44	Embedded System Using C	Ethnotech

S. No	Course Code	Course Title	Certified By
45	P23XXCX45	Embedded System with IoT / Arduino	Ethnotech
46	P23XXCX46	English for IT	Ethnotech
47	P23XXCX47	Plaxis	Ethnotech
48	P23XXCX48	Sketch Up	Ethnotech
49	P23XXCX49	Financial Planning, Banking and Investment Management	Ethnotech
50	P23XXCX50	Foundation of Stock Market Investing	Ethnotech
51	P23XXCX51	Machine Learning / Machine Learning for Medical Diagnosis	Ethnotech
52	P23XXCX52	IOT Using Python	Ethnotech
53	P23XXCX53	Creo (Modelling & Simulation)	Ethnotech
54	P23XXCX54	Soft Skills, Verbal, Aptitude	Ethnotech
55	P23XXCX55	Software Testing	Ethnotech
56	P23XXCX56	MX-Road	Ethnotech
57	P23XXCX57	CLO 3D	Ethnotech
58	P23XXCX58	Solid works	Ethnotech
59	P23XXCX59	Staad Pro	Ethnotech
60	P23XXCX60	Total Station	Ethnotech
61	P23XXCX61	Hydraulic Automation	Festo
62	P23XXCX62	Industrial Automation	Festo
63	P23XXCX63	Pneumatics Automation	Festo
64	P23XXCX64	Agile Methodologies	IBM
65	P23XXCX65	Block Chain	IBM
66	P23XXCX66	Devops	IBM
67	P23XXCX67	Artificial Intelligence	ITS
68	P23XXCX68	Cloud Computing	ITS
69	P23XXCX69	Computational Thinking	ITS
70	P23XXCX70	Cyber Security	ITS
71	P23XXCX71	Data Analytics	ITS
72	P23XXCX72	Databases	ITS
73	P23XXCX73	Java Programming	ITS
74	P23XXCX74	Networking	ITS
75	P23XXCX75	Python Programming	ITS
76	P23XXCX76	Web Application Development (HTML, CSS, JS)	ITS
77	P23XXCX77	Network Security	ITS & Palo alto
78	P23XXCX78	MATLAB	MathWorks
79	P23XXCX79	Azure Fundamentals	Microsoft
80	P23XXCX80	Azure AI (AI-900)	Microsoft
81	P23XXCX81	Azure Data (DP -900)	Microsoft
82	P23XXCX82	Microsoft 365 Fundamentals (SS-900)	Microsoft
83	P23XXCX83	Microsoft Security, Compliance and Identity (SC-900)	Microsoft
84	P23XXCX84	Microsoft Power Platform (PI-900)	Microsoft
85	P23XXCX85	Microsoft Dynamics Fundamentals 365 – CRM	Microsoft
86	P23XXCX86	Microsoft Excel	Microsoft
87	P23XXCX87	Microsoft Excel Expert	Microsoft
88	P23XXCX88	Securities Market Foundation	NISM
89	P23XXCX89	Derivatives Equinity	NISM
90	P23XXCX90	Research Analyst	NISM
91	P23XXCX91	Portfolio Management Services	NISM
92	P23XXCX92	Cyber Security	Palo alto

S. No	Course Code	Course Title	Certified By
93	P23XXCX93	Cloud Security	Palo alto
94	P23XXCX94	PMI – Ready	PMI
95	P23XXCX95	Tally – GST & TDS	Tally
96	P23XXCX96	Advance Tally	Tally
97	P23XXCX97	Associate Artist	Unity
98	P23XXCX98	Certified Unity Programming	Unity
99	P23XXCX99	VR Development	Unity

Annexure- C

AUDIT COURSES

Sl. No.	Course Code	Course Title
1	P23ACTX01	English for Research Paper Writing
2	P23ACTX02	Disaster Management
3	P23ACTX03	Sanskrit for Technical Knowledge
4	P23ACTX04	Value Education
5	P23ACTX05	Constitution of India
6	P23ACTX06	Pedagogy Studies
7	P23ACTX07	Stress Management by Yoga
8	P23ACTX08	Personality Development Through Life Enlightenment Skills
9	P23ACTX09	Unnat Bharat Abhiyan

ANNEXURE – 1 (B): UPDATED SYLLABUS

M.Tech – Electronics and Communication Engineering

Semester	Course Code	Course Title
I	P23ECT103	High Speed Electronics
II	P23VETC02	Embedded Processors

Semester	Course Code	Course Title
I	P23ECE101	Advanced Microprocessor and Interfacing
II	P23VEEC02	Internet of Things and its Implementation

Department	ECE	Programme: **M.Tech.- ECE**						
Semester	I	Course Category: **PC**			*End Semester Exam Type: **TE**			
Course Code	**P23ECT103**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**High Speed Electronics**	3	0	0	3	40	60	100

Prerequisite			
Course Outcome	On completion of the course, the students will be able to		BT Mapping (Highest Level)
	CO1	Understand the concept of Semiconductor Material with its Characteristics	2
	CO2	To explain about homo junction and its characteristics in FET, BJT	2
	CO3	Differentiate homo-junction and hetero-junction Devices	2
	CO4	Apply knowledge of Advanced Devices in High-Speed Application	2
	CO5	Understand various process of Fabrication and Characterization Techniques	2

Unit-I	**Semiconductor Material Characteristics**	**Periods: 09**
Review of Crystal Structure: Crystal structure of important semiconductors (Si, GaAs, InP) - electrons in periodic lattices - energy band diagram - carrier concentration and carrier transport phenomenon - electrical - optical - thermal and high field properties of semiconductors		CO1
Unit-II	**Homojunction Device**	**Periods: 09**
Homojunction Devices (BJT and FET): Structure - band diagram - operation - I–V and C–V characteristics (analytical expressions) - small signal switching models		CO2
Unit-III	**MOS Device**	**Periods: 09**
MOS Diode: Structure - band diagram - operation - C–V characteristics - effects of oxide charges - avalanche injection - high field effects and breakdown; Heterojunction Based MOSFET: Band diagram - structure - operation - I–V and C–V characteristics (analytical expressions) - MOSFET breakdown and punch through – sub-threshold current -scaling down; Alternate High k-dielectric Materials: HF–MOSFETs - SOI MOSFET - buried channel MOSFET - charge coupled devices		CO3
Unit-IV	**Advanced Device**	**Periods: 09**
HBT and HEMT Devices: AlGaAs/ GaAs, InP and SiGe based HBT and HEMT structure - band diagram - operation - I–V and C–V characteristics (analytical expressions) - small signal switching models - benefits of hetero-junction transistor for high speed applications		CO4
Unit-V	**Fabrication and Characterization Techniques**	**Periods: 09**
Crystal Growth and Wafer Preparation: Epitaxy - diffusion - ion implantation - dielectric film deposition and oxidization techniques - masking and lithography techniques (optical, e-beam and other advanced lithography techniques) - metallization - bipolar and MOS integration techniques - interface passivation techniques; Characterization Techniques: Four probe and hall effect measurement - I–V and C–V for dopant profile characterization and DLTS		CO5

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Textbooks

1. Nandita Das Gupta and Amitava Das Gupta, “Semiconductor Devices: Modeling and Technology”, Prentice Hall of India,2012.
2. M. S. Tyagi, “Introduction to Semiconductor Materials and Devices”, John Wiley and Sons, 2008.
3. M. J. Madou, Fundamentals of Microfabrication, 2nd Edition, CRC Press, 2011.
4. P. Bhattacharya, Semiconductor Optoelectronics Devices, 2nd Edition, PHI, 2009

Reference Books

1. S. M. Sze, “Physics of Semiconductor Devices”, 3rd edition, John Wiley and Sons,2007.
2. J. Singh, “Semiconductor Devices: Basic Principles”, John Wiley and Sons,2007.
3. J. P. McKelvey, Introduction to Solid State and Semiconductor Physics, Harper and Row and John Weathe Hill.
4. Cheng T. Wang, Ed., Introduction to Semiconductor Technology: GaAs and Related Compounds, John Wiley & Sons, 1990.
5. Donald A Neamen, Semiconductor Physics and Devices: Basic Principles, McGraw-Hill (1997) ISBN 0-256-24214-3

Web References

1. https://nptel.ac.in/courses/117104071/
2. https://cosmolearning.org/courses/high-speed-devices-circuits/
3. https://www.docsity.com/en/lecture-notes/subjects/high-speed-electron-devices/
4. https://www.researchgate.net/journal/International-Journal-of-High-Speed-Electronics-and-Systems-0129-1564
5. https://ieeexplore.ieee.org/document/6647520

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	1	1	1	-	-	1	-	3
2	2	1	2	1	-	-	1	-	3
3	2	1	2	1	-	-	1	-	3
4	2	2	2	1	-	-	1	-	3
5	2	2	1	1	-	-	1	3	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**ECE**	Programme: M.Tech. ECE						
Semester	**II**	Course Category: **PC**			*End Semester Exam Type: **TE**			
Course Code	**P23VETC02**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Embedded Processors**	3	0	0	3	40	60	100
(Common to M.Tech ECE and M.Tech – VLSI & ES)								
Prerequisite	**Microcontroller**							

Course Outcome		On completion of the course, the students will be able to	BT Mapping (Highest Level)
	CO1	Analyze the architectures of different Embedded Processors	3
	CO2	Identify an appropriate on chip peripherals for serial and parallel communication	2
	CO3	Examine the functions of ARM processors	3
	CO4	Develop real time applications using ARM processors	3
	CO5	Develop a firmware for embedded applications	3

s	**Introduction to Embedded Processors**	**Periods: 9**
Introduction to embedded processors– Compare Von Neumann architecture and Harvard architecture, RISC Vs CISC – System on Chip (SoC)-Introduction to SoC Architecture, An approach for SOC Design, System Architecture and Complexity. Processor Selection for SOC, Basic concepts in Processor Architecture, Overview of SOC external memory, Internal Memory, Scratchpads and Cache memory, SOC Memory System, Models of Simple Processor – memory interaction, SOC Standard Buses		CO1
Unit-II	**Embedded Processors on Chip Peripherals**	**Periods: 9**
Memory - Interrupts - I/O Ports-Timers & Real Time Clock (RTC), Watch dog timer - CCP modules - Capture Mode - Compare Mode-PWM Mode - Serial communication module - USART - SPI interface - I2C interface, Analog Comparator, Analog interfacing and data acquisition.		CO2
Unit-III	**ARM Processor**	**Periods: 9**
Architecture of ARM Controller – Registers, Pipeline organization 3 stage & 5 stage, Thumb mode of operation - D/A and A/D converter, sensors, actuators and their interfacing – Case study- Digital clock, Temperature sensing, Light sensing, Introduction to Internet of Things, smart home concepts		CO3
Unit-IV	**Real World Interfacing Using ARM Processor**	**Periods: 9**
Interfacing the peripherals to LPC2148: GSM and GPS using UART, on-chip ADC using interrupt (VIC), EEPROM using I2C, SD card interface using SPI, on-chip DAC for waveform generation.		CO4
Unit-V	**ARM Cortex Processors**	**Periods: 9**
Introduction to ARM CORTEX series, improvement over classical series and advantages for embedded system design. CORTEX A, CORTEX M, CORTEX R processors series, versions, features and applications, need of operating system in developing complex applications in embedded system, Firmware development for ARM Cortex, Survey of CORTEX M3 based controllers, its features and comparison		CO5

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Textbooks

1. F. Vahid and T. Givargis, “Embedded System Design: A Unified Hardware/Software Introduction”, Wiley India Pvt. Ltd., 2002.
2. Lyla B. Das, “Architecture, Programming and Interfacing of Low-power Processors ARM 7, Cortex-M”, Cengage, 1st Edition, 2017.

Reference Books

1. Andrew Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s Guide – Designing and Optimizing System Software”, ELSEVIER
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M”, Newness, ELSEVIER
3. Embedded Systems: Real-Time Interfacing to ARM Cortex-M Microcontrollers,2014, Jonathan W Valvano CreateSpace publications ISBN: 978-1463590154.

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1. LPC 214x User manual (UM10139): - www.nxp.com
2. LPC 17xx User manual (UM10360): - www.nxp.com
3. ARM architecture reference manual: - www.arm.com
4. http://processors.wiki.ti.com/index.php/HandsOn_Training_for_TI_Embedded_Processors
5. http://processors.wiki.ti.com/index.php/MCU_Day_Internet_of_Things_2013_Workshop

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	3	3	3	3	3	-	3	2	-
2	3	3	3	3	3	-	3	2	-
3	3	3	3	3	3	-	3	2	-
4	3	3	3	3	3	-	3	2	-
5	3	3	3	3	3	-	3	2	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	ECE	Programme: **M.Tech. - ECE**						
Semester	I	Course Category Code: **PE**				*End Semester Exam Type: **TE**		
Course Code	P23ECE101	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Advanced Microprocessor and Interfacing**	3	0	0	3	40	60	100

Prerequisite			
Course Outcome	**On completion of the course, the students will be able to**		**BT Mapping (Highest Level)**
	CO1	Explain advanced microprocessor architecture	**K2**
	CO2	Interpret modular programming concepts	**K2**
	CO3	Describe organization PIC16F877 microcontrollers	**K2**
	CO4	Interface peripheral devices with PIC16F877 Microcontrollers	**K3**
	CO5	Design and develop on Microcontroller Based system design	**K4**

Unit - I	**Advanced Microprocessor Architecture**	**Periods: 9**
Internal Microprocessor Architecture-Real mode memory addressing – Protected Mode Memory addressing –Memory paging - Data addressing modes – Program memory addressing modes – Stack memory addressing modes – Data movement instructions – Program control instructions- Arithmetic and Logic Instructions		**CO1**
Unit - II	**Modular Programming and its Concepts**	**Periods: 9**
Fundamental of high-level synthesis, Logic synthesis, Logic optimization and technology mapping, Lookup table technology mapping, Timing analysis, Timing optimization, Area optimization		**CO2**
Unit - III	**PIC Microcontroller**	**Periods: 9**
Architecture – memory organization – addressing modes – instruction set – PIC programming in Assembly & C –I/O port, Data Conversion, RAM & ROM Allocation, Timer programming		**CO3**
Unit - IV	**Peripheral of Pic Microcontroller**	**Periods: 9**
Timers – Interrupts, I/O ports- I2C bus-A/D converter-UART- CCP modules -ADC, DAC and Sensor Interfacing –Flash and EEPROM memories.		**CO4**
Unit - V	**Instructional Activity**	**Periods: 9**
Microcontroller based system design: Interfacing LCD Display – Keypad Interfacing - Generation of Gate signals for converters and Inverters - Motor Control – Controlling DC/ AC appliances – Measurement of frequency – Standalone Data Acquisition System.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Textbooks

1. Danny Causey, Rolin McKinlay and Muhammad Ali Mazidi 'PIC Microcontroller and Embedded Systems: Using Assembly and C for PIC18', Microdigitaled, 2016
2. Daniele Lacamera, 'Embedded Systems Architecture: Explore architectural concepts, pragmatic design patterns, and best practices to produce robust systems', Packt Publishing Limited, 2018
3. Marilyn Wolf 'PIC Embedded System Interfacing: Design for the Internet-of-Things (IoT) and Cyber-Physical Systems (CPS)', Elsevier Science & Technology, 2019

Reference Books

1. MykePredko, "Programming and customizing the 8051 microcontrollers", Tata McGraw Hill, 2001.
2. Rajkamal,". Microcontrollers-Architecture, Programming, Interfacing & System design",2nd edition, Pearson, 2012.
3. I Scott Mackenzie and Raphael C.W. Phan, "The Micro controller", Pearson, Fourth edition 2012
4. MS Mohanamba Govindappa,". PIC Microcontroller Programming with Sample Source Code", Createspace Independent Publishing Platform, 2018
5. William Jayden,". Interfacing PIC Microcontrollers to Peripherial", Createspace Independent Publishing Platform, 2017

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1. http:// www.nptel.iitm.ac.in
2. http:// www.microchip.com/design-centers/microcontrollers
3. https://learn.mikroe.com/
4. https://microcontrollerslab.com/pic-microcontroller-architecture/
5. https://nptel.ac.in/courses/117/104/117104072/

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	-	3
2	2	-	3	3	-	1	3	-	3
3	2	-	3	3	-	1	3	-	3
4	2	-	3	3	-	1	3	-	3
5	2	2	3	3	2	1	3	-	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**ECE**	Programme: **M.Tech. - ECE**						
Semester	**II**	Course Category: **PE**			*End Semester Exam Type: **TE**			
Course Code	**P23VEEC02**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Internet of Things and its Implementation**	**3**	**0**	**0**	**3**	40	60	100

Prerequisite	Nil

Course Outcome		**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1	Articulate the main concepts, key technologies, strength and limitations of IoT	K2
	CO2	Identify the architecture, infrastructure models of IoT	K2
	CO3	Analyze the networking and how the sensors are communicated in IoT.	K3
	CO4	Analyze and design different models for IoT implementation.	K3
	CO5	Identify and design the new models for market strategic interaction.	K3

Unit - I	**Introduction to Internet of Things & UML**	**Periods: 9**
Rise of the machines – Evolution of IoT – Web 3.0 view of IoT – Definition and characteristics of IoT – IoT Enabling Technologies – IoT Architecture -– Fog, Edge and Cloud in IoT – Functional blocks of an IoT ecosystem –Smart Objects and Connecting Smart Objects - IoT levels and deployment templates. Overview of Unified Modeling Language (UML). IoT Models: Domain Model, Information Model, Functional Model, Communication Model, Security Model.		**CO1**
Unit - II	**Middleware and Protocols of IOT**	**Periods: 9**
Middleware architecture of RFID,WSN,SCADA,M2M – Interoperability challenges of IoT-Protocols for RFID,WSN,SCADA,M2M- Zigbee, KNX, BACNet, MODBUS - Challenges Introduced by 5G in IoT Middleware(Technological Requirements of 5G Systems - Perspectives and a Middleware Approach Toward 5G (COMPaaS Middleware) – Resource management in IoT		**CO2**
Unit - III	**Communication and Networking**	**Periods: 9**
IoT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and LoRaWAN – Network Layer: IP versions, Constrained Nodes and Constrained Networks – Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks		**CO3**
Unit - IV	**IOT Implementation Tools**	**Periods: 9**
Introduction to Python, Introduction to different IoT tools, developing applications through IoT tools, developing sensor-based application through embedded system platform, Implementing IoT concepts with python, Implementation of IoT with Raspberry Pi		**CO4**
Unit - V	**Instructional Activity: Applications and Case Studies**	**Periods: 9**
Home automations - Smart cities – Environment – Energy – Retail – Logistics – Agriculture – Industry - Health and lifestyle – Case study.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Textbooks

1. Honbo Zhou, “Internet of Things in the cloud: A middleware perspective”, CRC press, 2012.
2. Vijay Madisetti and Arshdeep Bahga, “Internet of Things (A Hands-onApproach)”, VPT, 1st Edition, 2014.
3. Holler, Jan., Tsiatsis, Vlasios., Mulligan, Catherine., Karnouskos, Stamatis., Avesand, Stefan., Boyle, David. Internet of Things. Netherlands: Elsevier Science, 2014.

Reference Books

1. Pethuru Raj and Anupama C. Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press, 2017.
2. Constandinos X. Mavromoustakis, George Mastorakis, Jordi MongayBatalla, “Internet of Things (IoT) in 5G Mobile Technologies” Springer International Publishing Switzerland 2016.
3. Dieter Uckelmann, Mark Harrison, Florian Michahelles, “Architecting the Internet of Things” Springer-Verlag Berlin Heidelberg, 2011.

Web References

1. http://www.abouttheinternetofthings.com/category/iot-features/
2. https://connectedworld.com/
3. https://nptel.ac.in/courses/106/105/106105166/
4. https://lecturenotes.in/subject/370/internet-of-things-iot
5. https://www.codeproject.com/Learn/IoT/

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	3	3	-	1	3	-	3
2	2	-	3	3	-	1	3	-	3
3	2	-	3	3	-	1	3	-	3
4	2	-	3	3	-	1	3	-	3
5	2	2	3	3	2	1	3	-	3

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

ANNEXURE – 2 (A): CURRICULUM

M.Tech - VLSI and Embedded Systems

SRI MANAKULA VINAYAGAR
ENGINEERING COLLEGE
(An Autonomous Institution)

Puducherry

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

M.TECH.

VLSI AND EMBEDDED SYSTEMS

(REGULATIONS-2023)

CURRICULUM & SYLLABI

VISION AND MISSION OF THE INSTITUTE

VISION

To be globally recognized for excellence in quality education, innovation and research for the transformation of lives to serve the society.

MISSION

M1: Quality Education	To provide comprehensive academic system that amalgamates the cutting edge-technologies with best practices
M2: Research and Innovation	To foster value-based research and innovation in collaboration with industries and institutions globally for creating intellectuals with new avenues
M3: Employability and Entrepreneurship	To inculcate the employability and entrepreneurial skills through value and skill-based training
M4: Ethical Values	To instil deep sense of human values by blending societal righteousness with academic professionalism for the growth of society

VISION AND MISSION OF THE DEPARTMENT

VISION

Facilitate academic excellence and research among Electronics and Communication Engineers to meet the Global needs with high competence and ethical professionalism

MISSION

M1: Academic Excellence	To impart learning skills to meet the global challenges in the field of Electronics and Communication Engineering
M2: Research and Innovation	To provide excellence in research and innovation through multidisciplinary specialization
M3: Employability and Entrepreneurship	To enhance inter and intrapersonal skills among students to make them employable and entrepreneurs
M4: Ethics	To inculcate the significance of human values and professional skills to serve the society

PROGRAMME OUTCOMES (POs)

PO1: Exploration of Research:
An ability to independently carry out research/investigation and development work to solve practical problems.

PO2: Technical Skill:
An ability to write and present a substantial technical report/document.

PO3: Expertise in Academics:
Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Scholarship of Knowledge:
Acquire in-depth knowledge of specific discipline or professional area, including wider and global perspective, with an ability to discriminate, evaluate, analyze and synthesize existing and new knowledge, and integration of the same for enhancement of knowledge.

PO5: Usage of Modern Tools:
Create, select, learn and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex engineering activities with an understanding of the limitations.

PO6: Ethical Practices and Social Responsibility:
Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1: Technical Knowledge

Graduates will be able to develop an insightful combination of modern electronics and communication technology through technical knowledge.

PEO2: Research and Development

Enhance analytical and thinking skills to develop initiatives and innovative ideas for research and development, industry and societal requirements.

PEO3: Leadership

Inculcate the qualities of teamwork as well as social, interpersonal and leadership skills and adapt to the changing professional environments in the fields of engineering and technology

PEO4: Professional Ethics

Motivate graduates to become good human beings and responsible citizens for the overall welfare of the society.

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Domain Knowledge

Ability to understand the concepts in Electronics and Communication Engineering and to apply to different fields, such as Consumer Electronics, Communications, Signal Processing, etc.

PSO2: Embedded System Design

Ability to design a system based on the technical knowledge gained for embedded applications in electronics and communications engineering.

PSO3: Professional Competency

Ability to select cutting-edge engineering hardware and software tools to solve complex problems in Electronics and Communication Engineering

SEMESTER–I

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23MAT102	Applied Mathematics for VLSI	BS	2	2	0	3	40	60	100
2	P23VET101	Electronic Design Automation Tools	PC	3	0	0	3	40	60	100
3	P23VET102	FPGA Based System Design	PC	3	0	0	3	40	60	100
4	P23VET103	VLSI Design Techniques	PC	3	0	0	3	40	60	100
5	P23HSTC01	Research Methodology and IPR	HS	2	0	0	2	40	60	100
6	P23VEE1XX	Professional Elective - I	PE	3	0	0	3	40	60	100
Practical										
7	P23VEP101	VLSI Design Laboratory	PC	0	0	4	2	50	50	100
8	P23HSTC02	Technical Report Writing and Seminar	HS	0	0	4	2	100	0	100
Ability Enhancement Course										
9	P23VEC1XX	Certification Course – I	AEC	0	0	4	-	100	-	100
10	P23ACT10X	Audit Course - I	AEC	2	0	0	-	100	-	100
							21	**590**	**410**	**1000**

SEMESTER–II

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23VETC01	Advanced Digital System Design	PC	3	0	0	3	40	60	100
2	P23VETC02	Embedded Processors	PC	3	0	0	3	40	60	100
3	P23VETC03	Embedded System Design	PC	3	0	0	3	40	60	100
4	P23VET204	Low Power Digital VLSI Design	PC	3	0	0	3	40	60	100
5	P23VEE2XX	Professional Elective - II	PE	3	0	0	3	40	60	100
6	P23VEE2XX	Professional Elective - III	PE	3	0	0	3	40	60	100
Practical										
7	P23VEP202	Embedded System Design Laboratory	PC	0	0	4	2	50	50	100
8	P23HSTC03	Seminar on ICT a hands-on approach	HS	0	0	4	2	100	0	100
Ability Enhancement Course										
10	P23VEC2XX	Certification Course – II	AEC	0	0	4	-	100	-	100
11	P23ACT20X	Audit Course - II	AEC	2	0	0	-	100	-	100
Total							**22**	**590**	**410**	**1000**

SEMESTER–III

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Theory										
1	P23VEE3XX	Professional Elective - IV	PE	3	0	0	3	40	60	100
2	P23VEE3XX	Professional Elective - V	PE	3	0	0	3	40	60	100
3	P23VEE3XX	Professional Elective - VI	PE	3	0	0	3	40	60	100
Project Work										
7	P23VEW301	Project Phase - I	PA	0	0	12	6	50	50	100
8	P23VEW302	Internship	PA	0	0	0	2	100	0	100
Ability Enhancement Course										
10	P23VEC301	NPTEL / SWAYAM / MOOC	AEC	0	0	0	-	100	0	100
Total							**17**	**370**	**230**	**600**

SEMESTER–IV

Sl. No.	Course Code	Course Title	Category	Periods			Credits	Max. Marks		
				L	T	P		CAM	ESM	Total
Project Work										
1	P23VEW303	Project Phase - II	PA	0	0	24	12	50	50	100
Total							**12**	**50**	**50**	**100**

* Professional Elective Courses are to be selected from the list given in Annexure I
# Ability Enhancement Courses are to be selected from the list given in Annexure II
** Audit Courses are to be selected from the list given in Annexure III

BS – Basic Science
HS – Humanity Science
PC – Professional Core
PE – Professional Elective
PA – Project Work
C – Common Course
AEC – Audit Course
AEC – Ability Enhancement Course

Credit Distribution

Semester- I	Semester - II	Semester - III	Semester - IV	Total
21	**22**	**17**	**12**	**72**

Total number of credits required to complete M. Tech - VLSI AND Embedded Systems:	72 credits

Annexure – A

PROFESSIONAL ELECTIVE COURSES

Professional Elective –I (Offered in Semester I)		
Sl. No.	**Course Code**	**Course Title**
1	P23VEE101	Principles of ASIC Design
2	P23VEE102	VLSI Architecture
3	P23VEE103	Physical Design of VLSI
4	P23VEE104	Real Time Systems
5	P23VEE105	Analog IC Design
Professional Elective – II (Offered in Semester II)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC01	Design of Analog and Mixed VLSI Circuits
2	P23VEEC02	Internet of Things and its Implementation
3	P23VEE206	Modeling and Synthesis with Verilog HDL
4	P23VEE207	Advanced Embedded System
5	P23VEE208	Distributed Embedded Computing
Professional Elective –III (Offered in Semester II)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC03	System-on-Chip Design
2	P23VEE309	DSP Processor Architecture and Programming
3	P23VEE310	Design for Verification Using UVM
4	P23VEE311	Testing and Fault Diagnosis of VLSI Circuits
5	P23VEE312	Soft Computing
Professional Elective–IV (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC04	Real Time Operating System
2	P23VEEC05	Cloud computing and Distributed System
3	P23VEE313	VLSI Signal Processing
4	P23VEE414	High Speed Digital Design
5	P23VEE415	Computer Design Automation for VLSI Circuits
Professional Elective –V (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEEC06	Edge Computing
2	P23VEE416	CAD for VLSI Circuits
3	P23VEE217	Advanced Image Processing
4	P23VEE218	Hardware Software Co-Design
5	P23VEE519	Micro-Electromechanical Systems
Professional Elective–VI (Offered in Semester III)		
Sl. No	**Course Code**	**Course Title**
1	P23VEE520	Pervasive Devices and Technology
2	P23VEE521	Robotics and Automation
3	P23VEE622	Semiconductor Devices and Modeling
4	P23VEE623	VLSI for Wireless Communication
5	P23VEE624	RISC Processor Architecture and Programming

Annexure – B

ABILITY ENHANCEMENT COURSES

S. No	Course Code	Course Title	Certified By
1	P23XXCX01	Adobe Photoshop	Adobe
2	P23XXCX02	Adobe Animate	Adobe
3	P23XXCX03	Adobe Dreamweaver	Adobe
4	P23XXCX04	Adobe After Effects	Adobe
5	P23XXCX05	Adobe Illustrator	Adobe
6	P23XXCX06	Adobe InDesign	Adobe
7	P23XXCX07	Autodesk AutoCAD -ACU	Autodesk
8	P23XXCX08	Autodesk Inventor - ACU	Autodesk
9	P23XXCX09	Autodesk Revit - ACU	Autodesk
10	P23XXCX10	Autodesk Fusion 360 - ACU	Autodesk
11	P23XXCX11	Autodesk 3ds Max - ACU	Autodesk
12	P23XXCX12	Autodesk Maya - ACU	Autodesk
13	P23XXCX13	Cloud Security Foundations	AWS
14	P23XXCX14	Cloud Computing Architecture	AWS
15	P23XXCX15	Cloud Foundation	AWS
16	P23XXCX16	Cloud Practitioner	AWS
17	P23XXCX17	Cloud Solution Architect	AWS
18	P23XXCX18	Data Engineering	AWS
19	P23XXCX19	Machine Learning Foundation	AWS
20	P23XXCX20	Robotic Process Automation / Medical Robotics	Blue Prism
21	P23XXCX21	Advance Programming Using C	CISCO
22	P23XXCX22	Advance Programming Using C ++	CISCO
23	P23XXCX23	C Programming	CISCO
24	P23XXCX24	C++ Programming	CISCO
25	P23XXCX25	CCNP Enterprise: Advanced Routing	CISCO
26	P23XXCX26	CCNP Enterprise: Core Networking	CISCO
27	P23XXCX27	Cisco Certified Network Associate - Level 2	CISCO
28	P23XXCX28	Cisco Certified Network Associate- Level 1	CISCO
29	P23XXCX29	Cisco Certified Network Associate- Level 3	CISCO
30	P23XXCX30	Fundamentals of Internet of Things	CISCO
31	P23XXCX31	Internet of Things / Solar and Smart Energy System with IoT	CISCO
32	P23XXCX32	Java Script Programming	CISCO
33	P23XXCX33	NGD Linux Essentials	CISCO
34	P23XXCX34	NGD Linux I	CISCO
35	P23XXCX35	NGD Linux II	CISCO
36	P23XXCX36	Advance Java Programming	Ethnotech
37	P23XXCX37	Android Programming / Android Medical App Development	Ethnotech
38	P23XXCX38	Angular JS	Ethnotech
39	P23XXCX39	Catia	Ethnotech
40	P23XXCX40	Communication Skills for Business	Ethnotech
41	P23XXCX41	Coral Draw	Ethnotech
42	P23XXCX42	Data Science Using R	Ethnotech
43	P23XXCX43	Digital Marketing	Ethnotech
44	P23XXCX44	Embedded System Using C	Ethnotech
45	P23XXCX45	Embedded System with IoT / Arduino	Ethnotech
46	P23XXCX46	English for IT	Ethnotech

S. No	Course Code	Course Title	Certified By
47	P23XXCX47	Plaxis	Ethnotech
48	P23XXCX48	Sketch Up	Ethnotech
49	P23XXCX49	Financial Planning, Banking and Investment Management	Ethnotech
50	P23XXCX50	Foundation of Stock Market Investing	Ethnotech
51	P23XXCX51	Machine Learning / Machine Learning for Medical Diagnosis	Ethnotech
52	P23XXCX52	IOT Using Python	Ethnotech
53	P23XXCX53	Creo (Modelling & Simulation)	Ethnotech
54	P23XXCX54	Soft Skills, Verbal, Aptitude	Ethnotech
55	P23XXCX55	Software Testing	Ethnotech
56	P23XXCX56	MX-Road	Ethnotech
57	P23XXCX57	CLO 3D	Ethnotech
58	P23XXCX58	Solid works	Ethnotech
59	P23XXCX59	Staad Pro	Ethnotech
60	P23XXCX60	Total Station	Ethnotech
61	P23XXCX61	Hydraulic Automation	Festo
62	P23XXCX62	Industrial Automation	Festo
63	P23XXCX63	Pneumatics Automation	Festo
64	P23XXCX64	Agile Methodologies	IBM
65	P23XXCX65	Block Chain	IBM
66	P23XXCX66	Devops	IBM
67	P23XXCX67	Artificial Intelligence	ITS
68	P23XXCX68	Cloud Computing	ITS
69	P23XXCX69	Computational Thinking	ITS
70	P23XXCX70	Cyber Security	ITS
71	P23XXCX71	Data Analytics	ITS
72	P23XXCX72	Databases	ITS
73	P23XXCX73	Java Programming	ITS
74	P23XXCX74	Networking	ITS
75	P23XXCX75	Python Programming	ITS
76	P23XXCX76	Web Application Development (HTML, CSS, JS)	ITS
77	P23XXCX77	Network Security	ITS & Palo alto
78	P23XXCX78	MATLAB	MathWorks
79	P23XXCX79	Azure Fundamentals	Microsoft
80	P23XXCX80	Azure AI (AI-900)	Microsoft
81	P23XXCX81	Azure Data (DP -900)	Microsoft
82	P23XXCX82	Microsoft 365 Fundamentals (SS-900)	Microsoft
83	P23XXCX83	Microsoft Security, Compliance and Identity (SC-900)	Microsoft
84	P23XXCX84	Microsoft Power Platform (PI-900)	Microsoft
85	P23XXCX85	Microsoft Dynamics Fundamentals 365 – CRM	Microsoft
86	P23XXCX86	Microsoft Excel	Microsoft
87	P23XXCX87	Microsoft Excel Expert	Microsoft
88	P23XXCX88	Securities Market Foundation	NISM
89	P23XXCX89	Derivatives Equinity	NISM
90	P23XXCX90	Research Analyst	NISM
91	P23XXCX91	Portfolio Management Services	NISM
92	P23XXCX92	Cyber Security	Palo alto

S. No	Course Code	Course Title	Certified By
93	P23XXCX93	Cloud Security	Palo alto
94	P23XXCX94	PMI – Ready	PMI
95	P23XXCX95	Tally – GST & TDS	Tally
96	P23XXCX96	Advance Tally	Tally
97	P23XXCX97	Associate Artist	Unity
98	P23XXCX98	Certified Unity Programming	Unity
99	P23XXCX99	VR Development	Unity

**Any one course to be selected from the list*

Annexure - C

AUDIT COURSES

Sl. No.	Course Code	Course Title
1	P23ACTX01	English for Research Paper Writing
2	P23ACTX02	Disaster Management
3	P23ACTX03	Sanskrit for Technical Knowledge
4	P23ACTX04	Value Education
5	P23ACTX05	Constitution of India
6	P23ACTX06	Pedagogy Studies
7	P23ACTX07	Stress Management by Yoga
8	P23ACTX08	Personality Development Through Life Enlightenment Skills
9	P23ACTX09	Unnat Bharat Abhiyan

ANNEXURES – 2 (B) UPDATED SYLLABUS

M.Tech - VLSI and Embedded Systems

Professional Core Course

Semester	Course Code	Course Title
I	P23VET101	Electronic Design Automation Tools
II	P23VETC02	Embedded Processors

Elective Course

Semester	Course Code	Course Title
I	P23VEE105	Analog IC Design
II	P23VEE310	Design for Verification Using UVM
II	P23VEE311	Testing and Fault Diagnosis of VLSI Circuits

Department	**ECE**	Programme: **M.Tech. - VLSI & ES**						
Semester	**I**	Course Category: **PC**			*End Semester Exam Type: **TE**			
Course Code	**P23VET101**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Electronic Design Automation Tools**	3	0	0	3	40	60	100

Prerequisite	**VERILOG, VHDL**		
Course Outcome	**On completion of the course, the students will be able to**		BT Mapping (Highest Level)
	CO1	Understand Functional design and verification models.	3
	CO2	Synthesize circuits using HDL codes.	3
	CO3	Design circuits, IC design flow using PSPICE tool,	3
	CO4	Design Mixed signal design flow for integrated circuit design.	3
	CO5	Implement Microelectronics design using Electronic Design Automation (EDA) tools.	4
Unit-I	**Simulation Using HDL**		**Periods: 9**
Simulation-Types of Simulation, Logic Systems, Working of Logic Simulation, Cell Models, Delay Models, State Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation.			CO1
Unit-II	**Synthesis Using HDL**		**Periods: 9**
Verilog and Logic Synthesis, VHDL and Logic Synthesis, Memory Synthesis, FSM Synthesis, Memory Synthesis, Performance-Driven Synthesis. CAD Tools for Simulation and Synthesis: Modelsim and Leonardo Spectrum			CO2
Unit-III	**Circuit Design and Simulation Using PSPICE**		**Periods: 9**
Pspice Models for Transistors, A/D & D/A Sample and Hold Circuits etc., and Digital System Building Blocks, Design and Analysis of Analog and Digital Circuits Using PSPICE.			CO3
Unit-IV	**An Overview of Mixed Signal VLSI Design**		**Periods: 9**
Fundamentals of Analog and Digital Simulation, Mixed Signal Simulator Configurations, Understanding Modeling, Integration to CAD Environments.			CO4
Unit-V	**Instructional Activity**		**Periods: 9**
An Overview of High-Speed PCB Design, Design Entry, Simulation and Layout Tools for PCB, Introduction to OrCAD PCB Design Tools.			CO5

Lecture Periods: 45	Tutorial Periods: -	Practical Periods: -	Total Periods: 45

Textbooks

1. J.Bhaskar, “A Verilog Primer”, BSP, 2003.
2. J.Bhaskar, “A Verilog HDL Synthesis”, BSP, 2003.
3. M.H.RASHID, “SPICE FOR Circuits and ElectronicsUsing PSPICE”, (2/E) (1992) Prentice Hall.

Reference Books

1. M.J.S.SMITH, “Application-Specific Integrated Circuits”,(1997). Addison Wesley.
2. J.Bhaskar, “A VHDL Synthesis Primer”, BSP, 2003.

Web References

1. https://nptel.ac.in/courses/106105083
2. https://onlinecourses.swayam2.ac.in/aic20_sp59/preview
3. https://www.btechguru.com/courses--nptel----electronic-design-automation-video-lecture--cse--CS100413V.html
4. https://cosmolearning.org/courses/electronic-design-automation-544/
5. https://www.udemy.com/course/fpga-embedded-design-eda-tools/

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	2	1	2	-	1	3	2	-
2	2	2	1	2	-	1	3	2	-
3	2	2	1	2	-	1	3	2	-
4	2	2	1	2	-	1	3	2	-
5	2	2	1	2	2	1	3	2	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**ECE**	Programme: **M.Tech. VLSI & ES**						
Semester	**II**	Course Category: PC			*End Semester Exam Type: TE			
Course Code	**P23VETC02**	Periods/Week			Credit	Maximum Marks		
		L	**T**	**P**	**C**	**CAM**	**ESE**	**TM**
Course Name	**Embedded Processors**	3	0	0	3	40	60	100
(Common to M.Tech ECE and M.Tech – VLSI & ES)								
Prerequisite	**Microcontroller**							

Course Outcome		**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1	Analyze the architectures of different Embedded Processors	3
	CO2	Identify an appropriate on chip peripherals for serial and parallel communication	2
	CO3	Examine the functions of ARM processors	3
	CO4	Develop real time applications using ARM processors	3
	CO5	Develop a firmware for embedded applications	3

Unit-I	**Introduction to Embedded Processors**	**Periods: 9**
Introduction to embedded processors– Compare Von Neumann architecture and Harvard architecture, RISC Vs CISC – System on Chip (SoC)-Introduction to SoC Architecture, An approach for SOC Design, System Architecture and Complexity. Processor Selection for SOC, Basic concepts in Processor Architecture, Overview of SOC external memory, Internal Memory, Scratchpads and Cache memory, SOC Memory System, Models of Simple Processor – memory interaction, SOC Standard Buses		CO1
Unit-II	**Embedded Processors on Chip Peripherals**	**Periods: 9**
Memory - Interrupts - I/O Ports-Timers & Real Time Clock (RTC), Watch dog timer - CCP modules - Capture Mode - Compare Mode-PWM Mode - Serial communication module - USART - SPI interface - I2C interface, Analog Comparator, Analog interfacing and data acquisition.		CO2
Unit-III	**ARM Processor**	**Periods: 9**
Architecture of ARM Controller – Registers, Pipeline organization 3 stage & 5 stage, Thumb mode of operation - D/A and A/D converter, sensors, actuators and their interfacing – Case study- Digital clock, Temperature sensing, Light sensing, Introduction to Internet of Things, smart home concepts		CO3
Unit-IV	**Real World Interfacing Using ARM Processor**	**Periods: 9**
Interfacing the peripherals to LPC2148: GSM and GPS using UART, on-chip ADC using interrupt (VIC), EEPROM using I2C, SD card interface using SPI, on-chip DAC for waveform generation.		CO4
Unit-V	**ARM Cortex Processors**	**Periods: 9**
Introduction to ARM CORTEX series, improvement over classical series and advantages for embedded system design. CORTEX A, CORTEX M, CORTEX R processors series, versions, features and applications, need of operating system in developing complex applications in embedded system, Firmware development for ARM Cortex, Survey of CORTEX M3 based controllers, its features and comparison		CO5

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Textbooks

1. F. Vahid and T. Givargis, “Embedded System Design: A Unified Hardware/Software Introduction”, Wiley India Pvt. Ltd., 2002.
2. Lyla B. Das, “Architecture, Programming and Interfacing of Low-power Processors ARM 7, Cortex-M”, Cengage, 1st Edition, 2017.

Reference Books

1. Andrew Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s Guide – Designing and Optimizing System Software”, ELSEVIER
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M”, Newness, ELSEVIER
3. Embedded Systems: Real-Time Interfacing to ARM Cortex-M Microcontrollers,2014, Jonathan W Valvano CreateSpace publications ISBN: 978-1463590154.

Web References

1. LPC 214x User manual (UM10139): - www.nxp.com
2. LPC 17xx User manual (UM10360): - www.nxp.com
3. ARM architecture reference manual: - www.arm.com
4. http://processors.wiki.ti.com/index.php/HandsOn_Training_for_TI_Embedded_Processors
5. http://processors.wiki.ti.com/index.php/MCU_Day_Internet_of_Things_2013_Workshop

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	3	3	3	3	3	-	3	2	-
2	3	3	3	3	3	-	3	2	-
3	3	3	3	3	3	-	3	2	-
4	3	3	3	3	3	-	3	2	-
5	3	3	3	3	3	-	3	2	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**ECE**	Programme: **M.Tech. VLSI & ES**						
Semester	**First**	Course Category Code: **PE**			*End Semester Exam Type: **TE**			
Course Code	**P23VEE105**	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	**Analog IC Design**	**3**	**0**	**0**	**3**	**40**	**60**	**100**

Prerequisite	Basic Electrical Circuits, Signals and Systems, Analog Circuits	
Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Design amplifiers to meet user specifications	K3
	CO2 Analyze the frequency and noise performance of amplifiers	K4
	CO3 Design and analyze feedback amplifiers and one stage op amps	K4
	CO4 Design and analyze two stage op amps	K4
	CO5 Design and analyze current mirrors and current sinks with MOS devices	K4

Unit- I	**Single Stage Amplifiers**	**Periods: 9**
Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, designof Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.		**CO1**
Unit- II	**High Frequency and Noise Characteristics of Amplifiers**	**Periods: 9**
Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.		**CO2**
Unit- III	**Feedback And Single Stage Operational Amplifiers**	**Periods: 9**
Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.		**CO3**
Unit- IV	**Stability And Frequency Compensation of Two Stage Amplifier**	**Periods: 9**
Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage And Using Cascode Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, And Compensation Of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.		**CO4**
Unit- V	**Bandgap References**	**Periods: 9**
Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascode current source, design of high swing cascode sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Textbooks

1. Jacob Baker “CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3rdEdition, 2010.
2. Willey M.C. Sansen, “Analog Design Essentials”, Springer, 2006.

Reference Books

1. Behzad Razavi, “Design of Analog Cmos Integrated Circuits”, Tata Mcgraw Hill, 2001.
2. Grebene, “Bipolar and Mos Analog Integrated Circuit Design”, John Wiley & Sons, Inc.,2003.
3. Phillip E.Allen, Douglas R .Holberg, “Cmos Analog Circuit Design”, Oxford University Press, 2ndEdition, 2002.
4. http://www.ee.iitm.ac.in/vlsi/courses/ee5320_2021/start

Web References

1. https://archive.nptel.ac.in/courses/117/106/117106030/
2. https://onlinecourses.nptel.ac.in/noc22_ee15/preview
3. https://onlinecourses.nptel.ac.in/noc22_ee34/preview
4. https://www.nptelvideos.com/course.php?id=525
5. https://www.udemy.com/topic/analog-circuits/

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	2	-	-	2	-	-	1	-	-
2	2	-	-	2	-	-	1	-	-
3	2	-	-	2	-	-	1	-	-
4	2	-	-	2	-	-	1	-	-
5	2	-	-	2	2	-	1	-	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**ECE**	Programme: **M.Tech. VLSI & ES**						
Semester	**II**	Course Category Code: **PE**			*End Semester Exam Type: **TE**			
Course Code	**P23VEE312**	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	**Design for Verification Using UVM**	**3**	**0**	**0**	**3**	**40**	**60**	**100**

Prerequisite	Nil	
Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Understand the basic concepts of two methodologies UVM	**K2**
	CO2 Build actual verification components.	**K3**
	CO3 Generate the register layer classes.	**K3**
	CO4 Code testbenches using UVM.	**K3**
	CO5 Understand advanced peripheral bus testbenches.	**K3**

Unit-I	**Introduction**	**Periods: 9**
Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation		**CO1**
Unit-II	**Developing Reusable Verification Components**	**Periods: 9**
Modeling Data Items for Generation - Transaction-Level Components - Creating the Driver - Creating the Sequencer - Connecting the Driver and Sequencer -Creating the Monitor - Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation -Managing of Test-Implementing Checks and Coverage		**CO2**
Unit-III	**UVM Using Verification Components**	**Periods: 9**
Creating a Top-Level Environment- Instantiating Verification Components - Creating Test Classes -Verification Component Configuration - Creating and Selecting a User-Defined Test - Creating Meaningful Tests- Virtual Sequences- Checking for DUT Correctness- Scoreboards- Implementing a Coverage Model		**CO3**
Unit-IV	**UVM Using the Register Layer Classes**	**Periods: 9**
Using the Register Layer Classes - Back-Door Access -Special Registers -Integrating a Register-Model in a Verification Environment- Integrating a Register Model- Randomizing Field Values- Pre-Defined Sequences		**CO4**
Unit-V	**Assignment in Testbenches**	**Periods: 9**
Assignment, APB: Protocol, Test bench Architecture, Driver and Sequencer, Monitor, Agent and Env; Creating Sequences, Building Test, Design and Testing of Top Module.		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 09**

Textbooks

1. The UVM Primer, An Introduction to the Universal Verification Methodology, Ray Salemi,2013.
2. Chris Spear, Greg Tumbush," System Verilog for Verification: A Guide to Learning the Testbench Language Features"3rd edition, 2012.

Reference Books

1. Rosenberg, Sharon, and Meade, Kathleen. A Practical Guide to Adopting the Universal Verification Methodology (UVM) Second Edition. United Kingdom, Lulu.com, 2012.
2. Rosenberg, Sharon, and Meade, Kathleen A. A Practical Guide to Adopting the Universal Verification Methodology (UVM). United States, Cadence Design Systems, 2010.

Web References

1. https://www.chipverify.com/uvm/uvm-tutorial
2. https://verificationguide.com/uvm/uvm-testbench-architecture/
3. https://www.udemy.com/course/learn-ovm-uvm/
4. https://cse.iitpkd.ac.in/courses/cs5626-PreSilicon-Design-Verification-using-Formal-Property-Verification/
5. https://www.cadence.com/en_US/home/training/all-courses/82143.html

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	1	-	1	1	2	-	1	-	-
2	1	-	1	1	2	-	1	-	-
3	1	-	1	1	2	-	1	-	-
4	1	-	1	1	2	1	1	-	-
5	1	-	1	1	2	1	1	-	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5

Department	**VLSI & Embedded systems**	Programme: **M.Tech. VLSI & ES.**						
Semester	**II**	Course Category Code: **PC**			*End Semester Exam Type: **TE**			
Course Code	**P23VEE314**	Periods/Week			Credit	Maximum Marks		
		L	T	P	C	CAM	ESE	TM
Course Name	**Testing and Fault Diagnosis of VLSI Circuits**	**3**	**0**	**0**	**3**	**40**	**60**	**100**

Prerequisite	To understand the process of test generation, DFT architecture and fault diagnosis	
Course Outcome	**On completion of the course, the students will be able to**	BT Mapping (Highest Level)
	CO1 Interpret the different types of fault models	K2
	CO2 Generate test patterns to detect the fault in combinational circuits	K3
	CO3 Generate test patterns to detect the fault in sequential circuits	K3
	CO4 Design a circuit for testability	K3
	CO5 Infer the different measures of system diagnosable	K2

Unit-I	**Fault Modeling and Simulation**	**Periods: 9**
Defect, errors and faults- Functional versus structural testing-Levels of fault models- Single stuck at fault-Modeling circuits for simulation- Algorithms for true-value simulation- Algorithms for fault simulation- Statistical methods for fault simulation		**CO1**
Unit-II	**Test Generation of Combinational Circuits**	**Periods: 9**
Algorithms and representation- Redundancy identification- Testing as a global problem-Combinational ATPG algorithm-D-algorithm-PODEM-FAN-Test generation Systems-Test compaction.		**CO2**
Unit-III	**Test Generation of Sequential Circuits**	**Periods: 9**
ATPG for single clock synchronous circuits- Time-Frame expansion method-Simulation based sequential circuit.		**CO3**
Unit-IV	**Design for Testability**	**Periods: 9**
Testability –AdHoc design for testability techniques- Controllability and observability by means of scan registers- Generic scan-based design- Classical scan designs- Board level and system level DFT approaches-Boundary scan standards		**CO4**
Unit-V	**Logic Level Diagnosis**	**Periods: 9**
Basic concepts- Fault dictionary- Guided probe testing- Diagnosis by UUT reduction-Fault diagnosis for combinational circuits- Expert systems for diagnosis - Effect cause analysis- Diagnostic reasoning based on structure and behavior		**CO5**

Lecture Periods: 45	**Tutorial Periods: -**	**Practical Periods: -**	**Total Periods: 45**

Textbooks

1. Bushnell M.L. and Agrawal V.D., “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2nd Printing, 2005.
2. Liu, Ruey-wen. Testing and Diagnosis of Analog Circuits and Systems. United States, Springer US, 2012.

Reference Books

1. Abramovici, M., Breuer, M.A and Friedman, A.D., “Digital Systems and Testable Design”, Jaico Publishing House, 13th Impression, 2012.
2. Laung – Terng wang, Cheng – wen wu, Xidogingwen, “VLSI Testing Principles and Architectures: Design for Testability”, Morgan Kaufmann Publisher,2nd Reprint, 2013.

Web References

1. https://onlinecourses.nptel.ac.in/noc20_ee76/preview
2. https://nptel.ac.in/courses/117105137
3. https://archive.nptel.ac.in/courses/106/103/106103116/
4. https://archive.nptel.ac.in/content/storage2/courses/106103116/
5. https://archive.nptel.ac.in/content/storage2/courses/106103116/handout/mod1.pdf

* TE – Theory Exam, LE – Lab Exam

COs/POs/PSOs Mapping

COs	Program Outcomes (POs)						Program Specific Outcomes (PSOs)		
	PO1	PO2	PO3	PO4	PO5	PO6	PSO1	PSO2	PSO3
1	3	1	1	-	-	-	1	-	-
2	3	2	1	-	-	-	1	-	-
3	3	2	1	-	-	-	1	-	-
4	3	2	1	-	2	-	1	-	-
5	2	1	1	-	-	-	1	-	-

Correlation Level: 1 - Low, 2 - Medium, 3 – High

Evaluation Method

Assessment	Continuous Assessment Marks (CAM)					End Semester Examination (ESE) Marks	Total Marks
	CAT 1	CAT 2	Model Exam	Assignment*	Attendance		
Marks	10		15	10	5	60	100

**Assignment to be given from Unit-5